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an introduction to
Field Effect Transistors

fets

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An Introduction to Field Effect Transistors

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INTRODUCTION TO THE FIELD EFFECT TRANSISTOR

- 1.1 The family of field effect transistors provides the electronic engineer with the means by which he may accomplish almost every known circuit function. The following short list of applications indicates the versatility of the family, and this booklet describes briefly the basic design concepts relating to each topic.

AMPLIFIERS

- small signal
- low distortion
- high gain
- low noise
- selective
- d.c.
- high-frequency

SWITCHES

- chopper-type
- analog gate

CURRENT LIMITERS

VOLTAGE CONTROLLED RESISTORS

INTEGRATED CIRCUITS

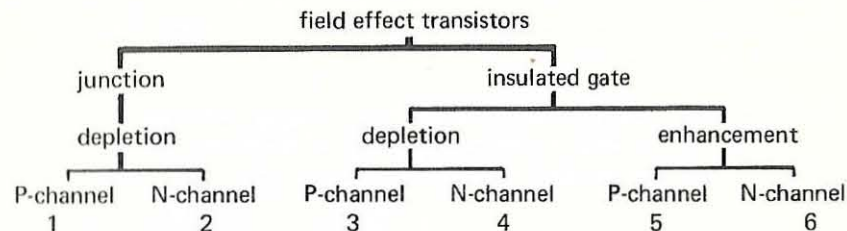
The very wide range of application of field effect transistors does not mean, however, that they will replace the more familiar bipolar types in every case. It simply means that their characteristics — which are very different from bipolar characteristics — often make possible the design of technically superior, and indeed cheaper, circuits. This comment applies to both linear and digital integrated circuits in addition to networks employing discrete devices. In fact, the state of the art currently allows a much greater packing density in large-scale-integrated circuits (LSI arrays) using field effect transistors than is possible for any competing bipolar process.

The family of field effect devices can be divided into two groups:

- (i) the Junction FET, or more simply the FET
- (ii) the Insulated Gate FET, or MOSFET, (metal-oxide-silicon-transistor).

As shown in the family tree on page 5, junction FET's, which are inherently depletion devices, are available in both N-channel and P-channel form. MOSFET's can exist as either depletion or enhancement devices, both of which are available in either N-channel or P-channel form. Of the resulting four categories, however, the P-channel MOSFET is the most common. The N-channel

depletion type is available, whilst the N-channel enhancement is just coming into use.



The two groups depend on somewhat different phenomena for their operation, and are introduced separately.

1.2 The Junction FET

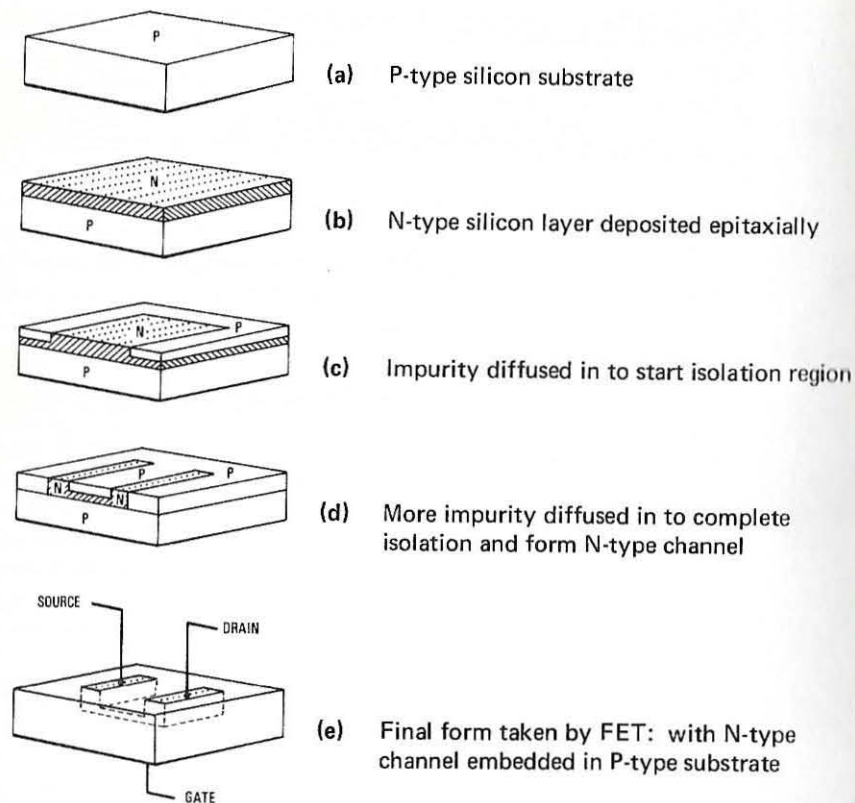
This transistor consists essentially of a channel of semiconductor material (usually silicon) through which a current flows, the magnitude of this current being controlled by a voltage applied to a gate, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the primary difference between the FET and the bipolar transistor: that because the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is not. In other words, the FET is inherently a high-input-resistance device — as against the comparatively low input resistance of the bipolar transistor.

Depending on whether the channel is doped with a donor impurity, giving N-type material, or with an acceptor impurity, giving P-type material, the channel current will consist of electrons or holes respectively. As would be expected, N-type channels have greater conductivity than P-type channels since electrons have a higher mobility than holes. This is substantiated by the fact that N-channel devices can be manufactured to exhibit lower channel resistance and higher transconductance than P-channel types. Hence the N-channel device is generally more efficient than its P-channel counterpart. These devices are particularly suited to fabrication by modern planar epitaxial methods, and Figure 1 illustrates this process in an idealized way. First, N-type silicon is deposited epitaxially onto mono-crystalline P-type silicon in such a manner as to maintain crystalline integrity. Then a layer of silicon dioxide is grown on the surface of the N-layer and a hole is etched therein so that acceptor-type impurity can be diffused through into the silicon. The resultant cross-section (shown in diagram c, Fig. 1) illustrates how a P-type annulus has been formed in the layer of N-type silicon. Diagram (d) shows how a further oxide-growing, etching and diffusing sequence can produce a channel of N-type material within the substrate.

Three ohmic (non-rectifying) contacts are made as shown in sketch (e), the two channel contacts being the SOURCE and DRAIN respectively. (For the

symmetrical geometry shown, it is immaterial which end of the channel is called the source and which the drain, but for more complex asymmetrical geometries this is not so). The sketch also shows how the N-channel is embedded in the P-silicon substrate in such a way that the GATE above the channel becomes part of this substrate.

Figure 1. *Idealized representation of the manufacture of an N-channel junction field effect transistor. Diagrams (a) to (d) are idealized cross sections; (e) idealized complete chip.*



To understand how the FET works, consider the idealized cross-sectional diagram of Figure 2 (a). If the gate is connected to the source then the full applied voltage V_{DS} appears between the gate and the drain; but because this is now a reverse-biased PN junction, practically no current will flow in the gate connection. However, the potential gradient so set up will form a depletion

layer, where almost all the free electrons present in the N-type channel will be swept away. Clearly the most depleted portion is in the high-field regions between the drain and the gate, and this depletion will reduce to zero at the gate-source region.

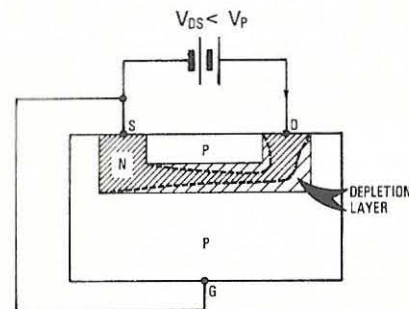


Figure 2a. *N-channel FET working below saturation ($V_{GS} = 0$). (Depletion shown only in channel region).*

Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current must fall as a progressively greater volume of silicon becomes depleted of free electrons. This means that there is a limit to the amount of current I_D which an increasing drain-source voltage V_{DS} can drive through the channel. This limiting current is given the symbol I_{DSS} , which means **D**rain to **S**ource current with the gate **S**hort-circuited. Figure 2 (b) shows the almost complete depletion of the channel under these conditions.

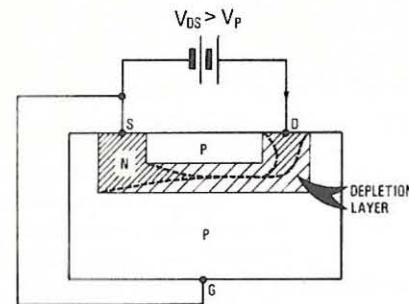


Figure 2b. *N-channel FET working in saturation region ($V_{GS} = 0$).*

Figure 2 (c) is a sketch of the output characteristic of an N-channel FET with the gate short-circuited to the source. The initial rise in I_D is related to the build-up of the depletion layer as V_{DS} increases, and the turn-over of the curve towards the limiting current I_{DSS} appears when I_D begins to be **pinched-off**. The physical meaning of this term is obvious from the diagrams, and leads to one definition of the **pinch-off voltage**, V_P , which is the value of V_{DS} at which the maximum current I_{DSS} flows. (This is actually a rather arbitrary definition, and more will be said about it in the next Chapter).

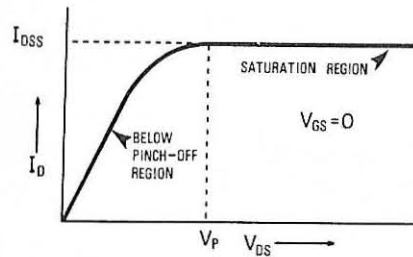


Figure 2c. Idealized output characteristic for $V_{GS} = 0$.

Now consider the case when $V_{DS} = 0$ and a negative voltage V_{GS} is applied to the gate. This situation is illustrated in Figure 3, from which it will be seen that a depletion layer has again built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a lower value than would be the case for $V_{GS} = 0$. In fact, at a value of $|V_{GS}| \geq |V_P|$ the channel current would be cut off almost entirely. This **cut-off voltage** is usually (and perhaps unfortunately) referred to as the **gate pinch-off voltage**, or simply the **pinch-off voltage**, and is also given the symbol V_P .

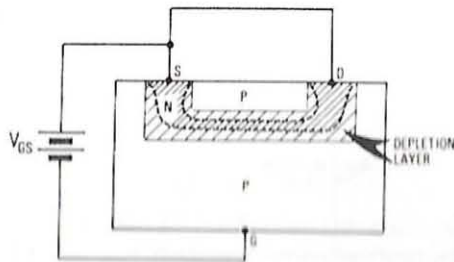


Figure 3. N-channel FET showing depletion layer due to gate-source voltage ($V_{DS} = 0$).

The consequences of the two mechanisms acting together is shown in Figure 4 (a), which gives a family of output characteristics. Figure 4 (b) relates these curves to the actual circuit arrangement, and shows how meters may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS} . Note that the direction of the arrow at the gate gives the direction of the current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.

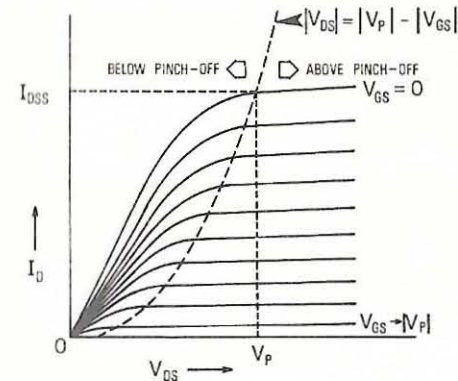
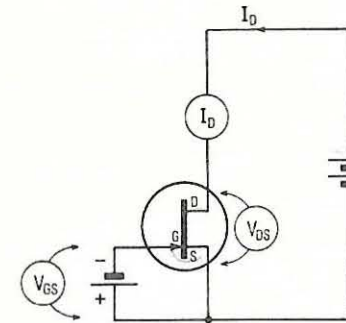


Figure 4. (a) Family of output characteristics for N-channel FET.



(b) Circuit arrangement for N-channel FET.

Returning to Figure 4 (a), the area of the graph below the pinch-off locus is called the triode or below pinch-off region; the area above is called the pentode, saturation, or pinch-off region. Later it will be seen how the FET can act as a voltage-dependent resistor or a low-level switch in the triode region; and as an amplifier in the saturation region. For the present it is sufficient to observe that below saturation, both V_{GS} and V_{DS} control the channel current, whereas in the saturation region V_{DS} has little effect, and V_{GS} is essentially in control of I_D .

The P-channel FET works in precisely the same manner as the N-channel, except that the channel current is due to hole movement. Consequently all the applied polarities are reversed, and their directions, along with the direction of current flow; as shown in Figure 5 (a). Sketched in Figure 5 (b) are the output characteristics of the P-channel FET, which, like those for the N-channel type, have been drawn in the correct quadrant in order to stress the current directions and polarities involved.

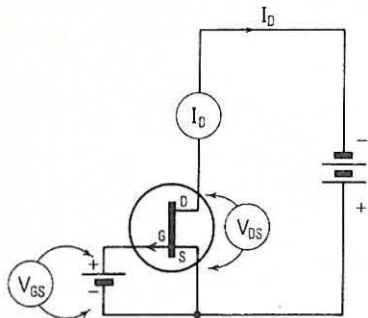
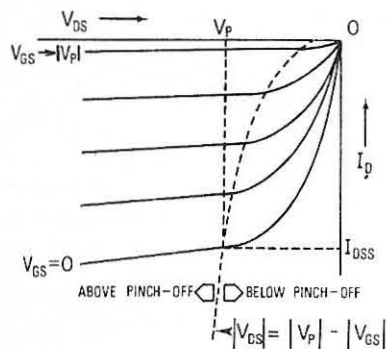


Figure 5. (a) Circuit arrangement for P-channel FET.



(b) Family of output characteristics for P-channel FET.

Some devices are manufactured using the planar diffusion sequence depicted in Figure 6, which is self-explanatory.

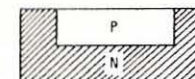
Summarizing, it can be said that the junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS} . When V_{DS} is greater than V_p , then the channel current is controlled largely by V_{GS} alone; and because V_{GS} is applied to a reverse-biased junction, the resultant gate current

is extremely small. In this sense, the N-channel FET is analogous to the thermionic pentode, and, as will be shown later, can be connected as an amplifier like the pentode.

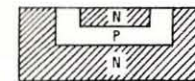
The P-channel junction FET behaves in a similar manner, but with the direction of current flow and both voltage polarities reversed. There is no good analogy with a thermionic tube here unless it is postulated that somewhere an anti-matter galaxy exists wherein positrons take the place of electrons, and anodes are biased negatively!



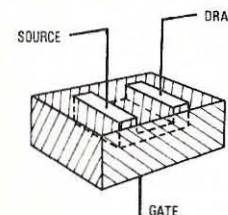
(a) N-type silicon substrate



(b) Acceptor impurity diffused in to form P-type silicon island



(c) Donor impurity diffused in to form second N-region, leaving a P-type channel



(d) Final form taken by P-channel FET

Figure 6. Idealized fabrication sequence for planar diffused P-channel FET.

1.3 The Insulated-Gate FET (or MOSFET)

The MOSFET depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate electrode

may simply be insulated from the channel by a thin layer of silicon-dioxide, as shown in Figure 7 (a). Although the bottom of the insulating layer is in contact with the P-type silicon substrate the physical processes occurring at this interface (bending of the Fermi levels) dictate that free electrons accumulate near this interface, spontaneously forming an N-type channel. This means that a conducting path exists between the diffused N-type source and drain regions, and furthermore, that the MOSFET will behave in a similar manner to the N-channel junction FET when a voltage of the correct polarity is applied to the channel (as in Figure 7 b).

The output characteristics of the device appear as in Figure 7 (c), but because there is no junction involved, V_{GS} can be reversed without engendering a gate current: that is, the gate can be made positive with respect to the source as well as negative. Under these circumstances yet more free electrons will be attracted to the channel region, and I_D will become **greater** than I_{DSS} . This mode of operation is represented by the upper members of the family of output characteristics.

Because the application of a negative gate voltage causes the channel to be depleted of free electrons — so reducing I_D — the device is called an **N-channel depletion-type MOSFET**. Note that since the insulating layer is usually silicon dioxide, the terms MOST and MOSFET are often used: but as fabrication using other insulating layers such as silicon nitride is feasible, the term IGFET would be more generic.

Returning to Figure 7 (b), it will be noticed that the MOSFET symbol used is descriptive of the device itself in that (a) the gate is removed from the channel, showing that a junction is not present, and (b) the polarity is indicated by the arrow defining the direction in which current would flow if the channel-substrate junction were forward-biased. (Notice that this arrow uses the same convention as for the N-channel junction FET). Later it will be shown that for some purposes the substrate will be biased rather than left floating as in Figure 7 (b).

The foregoing discussion has established that the depletion MOSFET is a **normally-ON** device — that is, when $V_{GS} = 0$, a conducting path exists between source and drain. For many purposes a **normally-OFF** device would be useful, and this leads to the concept of the **enhancement MOSFET**, so called because an increasing voltage applied to the gate will (if of the correct polarity) enhance channel conduction and depletion will never occur, I_D being zero when $V_{GS} = 0$.

The realization of such a device is illustrated (again ideally) in Figure 8 (a). Here, acceptor impurity has been diffused into an N-type silicon chip to form P-type source and drain regions, so that a PN junction exists between each of these and the substrate. Between the source and drain no conducting channel exists for, irrespective of the sense in which a drain-source voltage is applied, one of the PN junctions will inevitably be reverse-biased. If now a negative

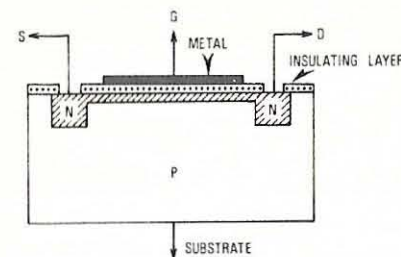


Figure 7a. Idealized cross-section through an N-channel depletion-type MOSFET

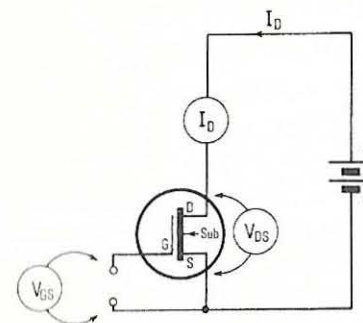


Figure 7b. Circuit arrangement for N-channel depletion MOSFET.

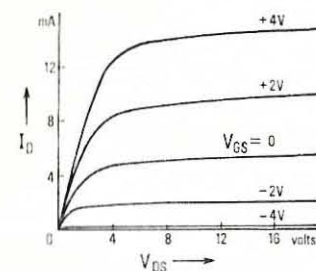


Figure 7c. Family of output characteristics for the Siliconix 2N3631 N-channel depletion MOSFET.

voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layers of the substrate, so producing a P-type channel. In other words, hole conduction becomes possible, and is progressively enhanced as V_{GS} increases negatively.

This situation is demonstrated by the family of output characteristics in Figure 8 (c). The normally-OFF property of the P-channel enhancement MOSFET is reflected in the symbol of Figure 8 (b), where the channel is represented by the broken (open circuit) line. This latter symbol, though logical, and approved by the I.E.E.E., is often ignored by manufacturers.

A symbol which is simpler to draw often appears in data sheets, and the user is expected to be sufficiently familiar with the technology to be undeterred by this confusing practice. The P-channel enhancement MOSFET is currently the most popular member of the family in general use, and is in fact the basic element in large-scale integrated circuits.

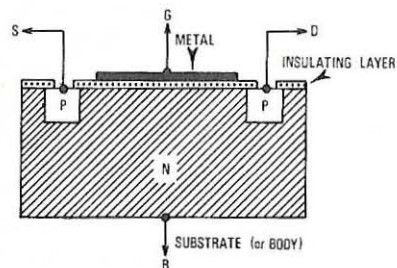


Figure 8a. *Idealized cross-section through a P-channel enhancement MOSFET.*

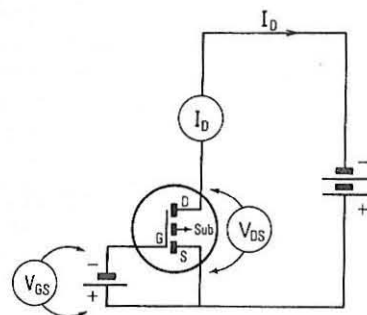


Figure 8b. *Circuit arrangement for P-channel enhancement MOSFET.*

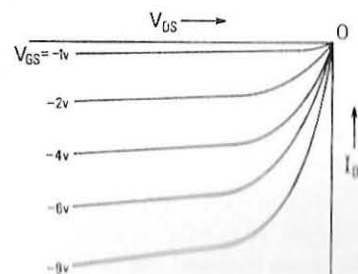


Figure 8c. *Family of output characteristics for a P-channel enhancement MOSFET.*

The idealized cross-sectional diagram of Figure 8 (a) may be used to illustrate the mechanism by which the characteristics of Figure 8 (c) come about. If a constant (negative) gate voltage, $V_{GS}(K)$, is applied, then a P-channel and an essentially uniform depletion layer will be induced as represented in Figure 8 (d).

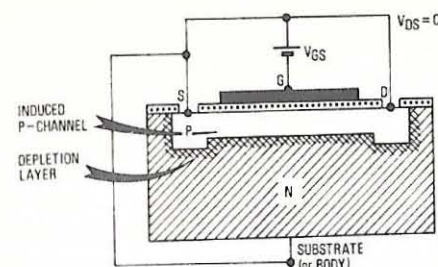


Figure 8d.

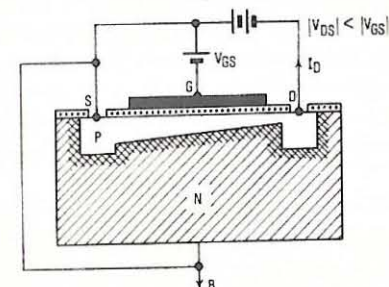


Figure 8e.

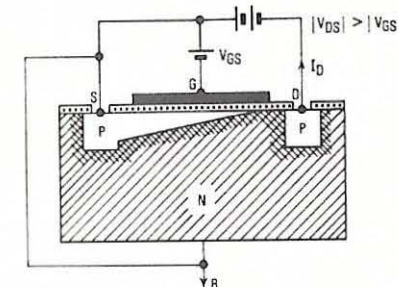


Figure 8f.

Idealized approach of pinch-off,
(d) $V_{DS} = 0$, (e) $|V_{DS}| < |V_{GS}|$, (f) $|V_{DS}| > |V_{GS}|$

If now a negative drain voltage V_{DS} is applied, a current I_D flows out of the drain. If $|V_{DS}|$ increases, $|I_D|$ also increases; but the voltage between the drain and gate decreases, so that the thickness of the channel at the drain end is reduced as indicated in Figure 8 (e). Therefore the curve of I_D versus V_{DS} begins to bend over (as shown in Figure 8 (c)), and will eventually reach a limiting value when $V_{DS} = V_{GS}$ and the channel becomes pinched-off. This situation is represented by Figure 8 (f).

Different values of V_{GS} give rise to different limiting values of I_D , so that the characteristic family of output curves shown in Figure 8 (c) is realized.

The depletion-type MOSFET characteristics also come about for the reasons described above except that members of the output characteristic family also exist for V_{GS} values of zero or reversed polarity.

In principle it is possible to manufacture the remaining two members of the MOSFET family — the P-channel depletion and the N-channel enhancement types. Because of the spontaneous formation of an N-channel at a silicon/silicon-dioxide interface, however, the processes involved become difficult. Though these types are obtainable, at the time of writing they are comparatively rare.

1.4 Summary

In this chapter a purely qualitative description of the family of six field effect transistors has been given. It is recognized that at first reading the properties and characteristics of the different types may be somewhat confusing, and the next chapter will therefore seek to tabulate them in terms of their gate-voltage versus drain-current performance, or transconductance curves, and these will be simply related to the symbols used for the various devices.

Chapter 2

CHARACTERISTICS, PARAMETERS AND TOLERANCES OF FIELD EFFECT TRANSISTORS

2.1 The Transconductance Curves of the Junction FET

A large proportion of field effect transistor applications including linear amplification involve operation in the saturation (or pinched-off) region of the output characteristics where V_{DS} has but little effect, and the gate voltage V_{GS} is in almost sole control of the channel current I_D . Under these circumstances it is entirely valid to characterize the FET in terms of the relationship between I_D and V_{GS} ; that is, by means of the transconductance curve.¹

Figure 9 illustrates transconductance curves for the two classes of junction FET,

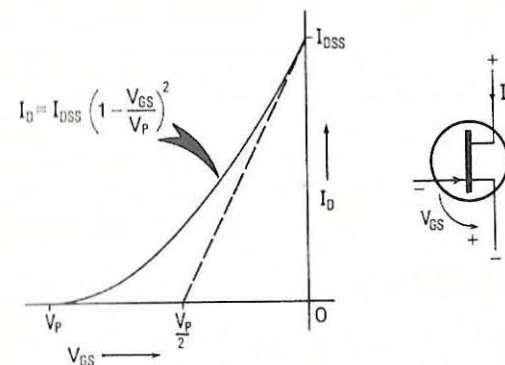


Figure 9a. Transconductance curves for an N-channel FET.

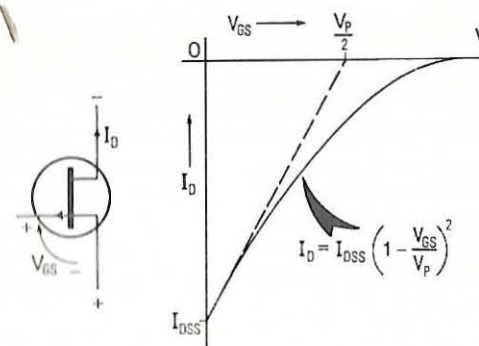


Figure 9b. Transconductance curves for a P-channel FET.

and does so in the correct quadrants so that the polarities of the applied voltages correspond to the signs of V_{GS} and I_D on the graphs. Here the convention is that currents into the FET are considered positive, and currents out of the FET are considered negative. For example, I_D for the N-channel FET is positive, whereas the source current I_S would be negative.

The transconductance curve is very important from the circuit design point of view because not only is it useful in determining the bias, or quiescent conditions under which the FET should operate, but its slope at the working point immediately gives the transconductance, g_{fs} . This is defined as the ratio of the small change in channel current to the small change in gate-source voltage which produces it. To extract this parameter, the equation to the transconductance curve must be known, and in the case of junction FET's, this is simply a square law:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \quad \dots (2.1)$$

(Actually, the index may be anything between 1.9 and 2.1, but for most practical purposes 2 is a satisfactory approximation.)

Differentiating I_D with respect to V_{GS} gives the transconductance at any working point:

$$g_{fs} = \frac{dI_D}{dV_{GS}} = -\frac{2 I_{DSS}}{V_P} \left[1 - \frac{V_{GS}}{V_P} \right] \quad \dots (2.2)$$

and in particular, where the transconductance curve meets the y-axis at $V_{GS} = 0$, this becomes:

$$g_{fso} = -\frac{2 I_{DSS}}{V_P} \quad \dots (2.3)$$

This is a parameter which is normally given on FET data sheets, and to obtain g_{fs} at any working point, it is necessary only to use a simple relationship derived from equations 2.2 and 2.3:

$$g_{fs} = g_{fso} \left[1 - \frac{V_{GSQ}}{V_P} \right] \quad \dots (2.4)$$

Where V_{GSQ} is the quiescent, or bias value of V_{GS} .

Notice that when numerical values, along with their proper signs, are inserted into the foregoing equations, g_{fs} always turns out to have a positive value, irrespective of the polarity of the FET. This is simply an expression of the fact that the transconductance curves rise from left to right — that is, they both have positive slopes. As will be seen later, this is not a purely academic point; when the characteristics of all six devices in the FET family are first being considered, much confusion can arise if sign conventions are ignored.

The square law form of the transconductance curve given in equation 2.1 is a very close approximation near $I_D = I_{DSS}$, but it becomes progressively less accurate as I_D becomes smaller. However, it does lead to a good definition of V_P , because, if equation 2.3 is re-written in the form:

$$g_{fso} = \frac{-I_{DSS}}{V_P/2}$$

it can be seen that this is the equation to a straight line whose slope is g_{fso} (where $I_D = I_{DSS}$) and which cuts the x-axis at $V_{GS} = \frac{1}{2}V_P$. Hence, V_P is precisely defined.

Although this result does lead to an a.c. method of measuring V_P , most manufacturers use a simpler d.c. method, and define V_P as that gate voltage which reduces I_D to some specific low value (often 1nA) at a stated value of V_{DS} . The value given by this method is not too far removed from that which would have resulted from a more valid measurement.

Also, the data sheet value for I_{DSS} is usually based on a measurement taken not at the 'knee' of the curve, as implied by Figures 2, 4 and 5, pages 7-10 but at some realistic value of V_{DS} . Obviously, to operate a FET near the 'knee' of its output curve would be quite unusual, because it would be working neither in the triode nor the saturation regions. It is therefore more reasonable to quote I_{DSS} at some point well into the saturation region where it will be most useful to the circuit designer.

Reference to the data sheet for the Siliconix E102 N-channel FET, for example, will demonstrate the foregoing points. Here,

$$V_P \text{ (at } V_{DS} = 20V \text{ and } I_D = 10nA) \\ = -0.8V \text{ (min.) to } -4.0V \text{ (max.)}$$

and

$$I_{DSS} \text{ (at } V_{DS} = 20V) = 0.9mA \text{ (min.) to } 4.5mA \text{ (max.)}$$

Also,

$$g_{fs} \text{ (at } V_{DS} = 20V \text{ and } V_{GS} = 0) = 1000 \mu mhos \text{ (min.)}$$

Notice that these three values imply the existence of tolerances; that is, ranges within which the quoted parameters are guaranteed to lie when the specified operating conditions are met. From the values of V_P and I_{DSS} given above, it is possible to draw a pair of transconductance curves which will define the upper limit and the lower limit FET's in the E102 class. This has been done in Figure 10.

The data sheet values V_P (min) and V_P (max) are quoted at a very low value of I_D (1nA), which is useful where switching calculations are involved. This leads to some slight inaccuracy in biasing calculations for linear amplifiers however, as

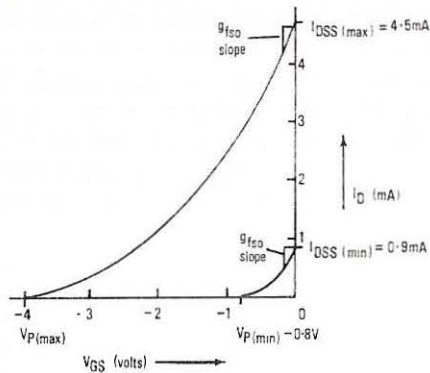


Figure 10. Limiting transconductance curves for the Siliconix E102 N-channel FET.

the best fit of the square-law theoretical transconductance curve will be found to occur if V_p is measured at

$$I_D \approx \frac{I_{DSS}}{100} \quad \text{— an approximation of which is true for most FET's.}$$

It is fortunate that, for reasons connected with the physical geometry of FET's a unit having a high I_{DSS} will also have a high V_p and vice versa, because it means that the limiting transconductance curves will never intersect. As demonstrated in Figure 10, it is possible to draw two such curves for a given FET and know that all FET's of that type number will exhibit transconductance curves between those limits. The next chapter will show how this presentation leads to a very simple method for bias circuit design.

Because the junction would be forward-biased if V_{GS} were made positive for N-channel or negative for P-channel FET's, the transconductance curve must stop when it meets the y-axis. However, knowing that a silicon PN junction will not begin to conduct until a few hundred millivolts has been applied in the forward direction, it is possible to allow V_{GS} to forward-bias the junction up to about two hundred millivolts if the design would be facilitated by so doing.

Conversely, the value of V_{GS} in the normal reverse direction may be increased only until the breakdown voltage of the junction is approached. This limiting voltage is termed BV_{GSS} , which means Breakdown Voltage from Gate to Source with the drain Short-circuited.

2.2 Output Characteristics for the Junction FET

A family of output characteristics for the Siliconix 2N2608 P-channel FET is reproduced in Figure 11. Notice that they are drawn in the first quadrant, but that the numerical values of I_D and V_{DS} are given negative signs. This is an alternative presentation very commonly found in data sheets.

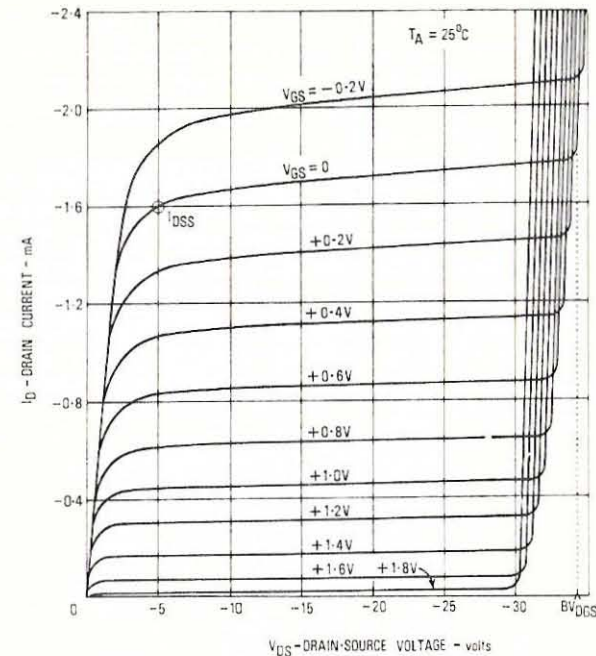


Figure 11. Output characteristics for the Siliconix 2N2608 P-channel FET.

Notice also that the upper characteristic is relevant to a **forward** gate voltage of -200mV . This illustrates the point made in section 2.2 that a small amount of forward gate bias is tolerable if called for in the circuit design.

Although the channel current of a FET is self-limiting at little more than I_{DSS} , it will suffer a catastrophic rise, possibly leading to destruction of the device, if a voltage in excess of the breakdown voltage BV_{DSS} is applied. The occurrence of such an event is clearly demonstrated by the sudden rise in I_D at the right-hand end of the family of output characteristics.

The mechanism involved here is actually that of a reverse voltage breakdown of the junction itself, as the term BV_{DSS} implies that the gate is short-circuited to the source. That is, $BV_{DSS} = BV_{DSX}$. The breakdown voltage for any other gate voltage is termed BV_{DSX} , and this voltage must then be specified.

The incremental slope at any point on an output characteristic is termed r_{ds} or its reciprocal g_{os} . That is,

$$r_{ds} = \frac{\delta V_{DS}}{\delta I_D} \quad \text{and} \quad g_{os} = \frac{\delta I_D}{\delta V_{DS}}$$

Manufacturers have arbitrarily elected to refer mainly to r_{ds} when considering triode region operation, and g_{os} when considering saturated operation. In the saturation regions, r_{ds} is obviously very large, because I_D is almost (but not quite) independent of V_{DS} . In the triode regions, however, I_D changes markedly with V_{DS} , so that r_{ds} becomes small.

It is in the triode region that the FET acts as a voltage controllable resistance, which is apparent from Figure 4 (a) Page 9, where the output characteristics will be seen to have slopes which depend on the values of V_{GS} . Figure 12 (a) shows these differing slopes in the region close to the origin where V_{DS} is very small. It also reflects the bi-directional nature of a symmetrical FET, for providing that the junction does not become significantly forward-biased, V_{DS} may be applied in either sense. Note that near the origin, before the characteristics turn over, the incremental channel resistance r_{ds} has the same values as the d.c. resistance r_{DS} .

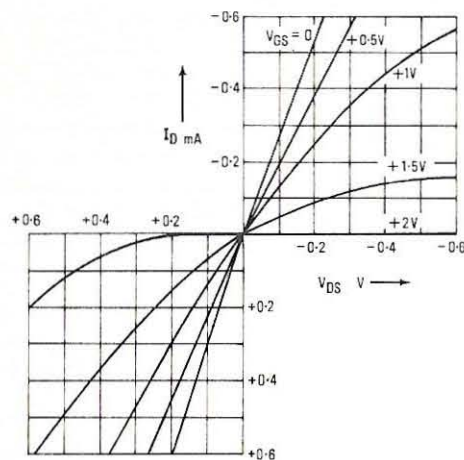


Figure 12. (a) Low-level bidirectional output characteristics for the Siliconix 2N2609 P-channel FET.

The values of r_{DS} near the origin are plotted in Figure 12 (b), from which it will be seen that in the case of the Siliconix 2N2609, for example, the channel resistance can vary from a few hundreds of ohms to many megohms. It is this property which is put to use in low-level chopper FET's and also in voltage-controlled-resistor types, both of which will be treated in detail later in the handbook.

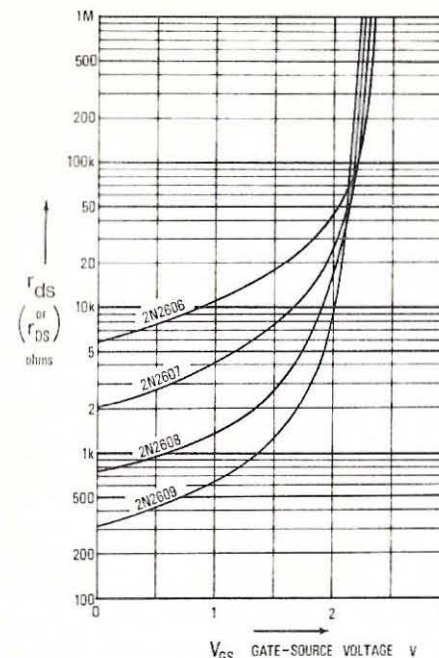


Figure 12. (b) Variation of incremental channel resistance r_{ds} with gate voltage V_{GS} .

2.3 Leakage currents and temperature effects in junction FET's.

Although a reverse-biased PN junction blocks current flow very efficiently, a small leakage current does appear due to the movement of thermally generated minority carriers. That is, normal thermal agitation produces a few free electrons in the P-region and a few free holes in the N-region. These charge carriers are accelerated across the junction by the electric field and so constitute a small leakage current.

Figure 13 (a) shows how I_{GSS} , the reverse Gate-to-Source current with the drain Short-circuited, is measured. I_{GSS} is made up of two current components, I_{DG} and I_{SG} , but if either the drain or the source is left open-circuited, the resultant currents become I_{GSO} and I_{GDO} respectively. These are slightly different from I_{DG} and I_{SG} because in the short-circuited case there is a contribution from each end of the channel.⁴

If the reverse gate voltage is increased beyond V_p so that the FET is cut off, then only a very small channel-gate leakage current, $I_{D(off)}$, flows. This is shown in Figure 13 (d). $I_{D(off)}$ is a measure of the 'goodness' of a FET switch.

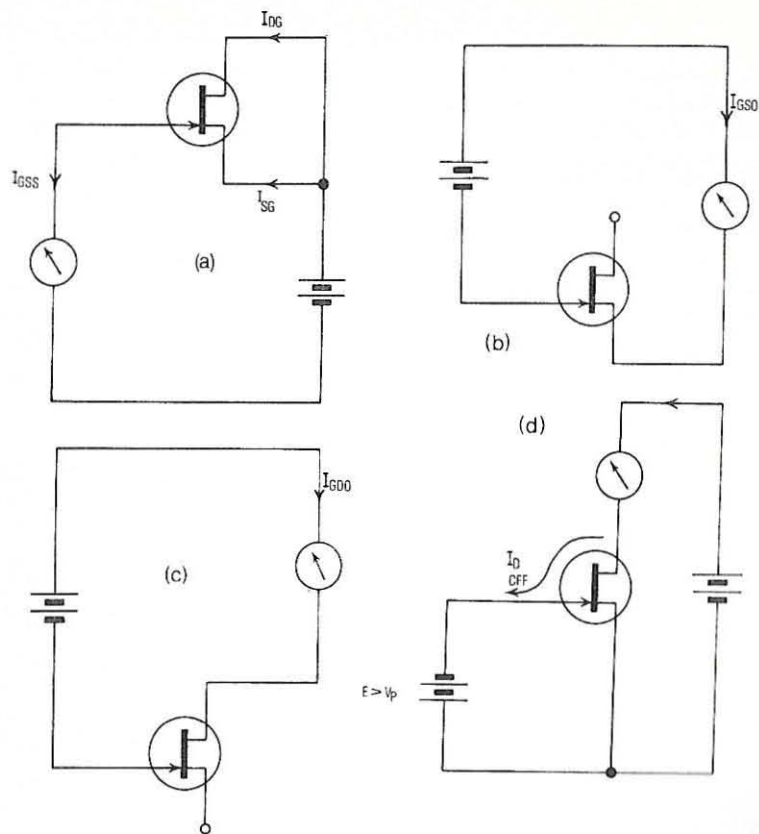


Figure 13 Measurement of leakage currents: (a) I_{GSS} , (b) I_{GSO} , (c) I_{GDO} , and (d) $I_{D(off)}$.

Returning to gate leakage currents, it is clear that because minority carrier generation is a thermal phenomenon, I_{GSS} should be proportional to temperature. This is in fact so, and a typical curve of I_{GSS} versus temperature is given in Figure 14. I_{GSS} is proportional to $\sqrt{V_{GS}}$, and is logarithmically dependent upon the temperature. This latter point means that a device which exhibits a very small leakage at room temperature may nevertheless allow an embarrassingly high I_{GSS} to flow at temperatures approaching 100°C . For approximate calculations it can be assumed that I_{GSS} doubles for every 11°C temperature rise.

Using the normal convention, I_{GSS} will be positive for a P-channel FET, and negative for an N-channel FET, but because the current direction is so obvious, the convention is rarely used in this context.

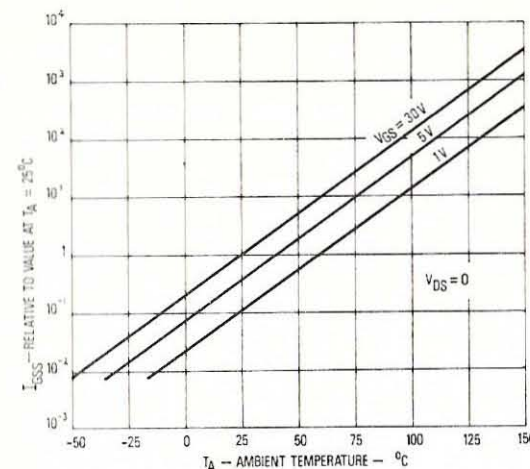


Figure 14. Variation of gate leakage current with temperature for a typical junction FET.

In actual practice, the gate leakage current of real interest is that which flows when the FET is working under its designed operating conditions, and it is for this reason that I_G is often quoted for specific values of V_{DG} and I_D . For N-channel FET's in particular, I_G at first rises slowly with increasing drain voltage, then increases very rapidly.²³ For most devices the turn-over occurs in the region where $V_{DG} \approx 20$ volts, and this is observed to be higher for elevated temperatures. It is thought that this phenomenon is due to carriers in the channel being accelerated by high fields sufficiently to generate hole-electron pairs by collision processes.

Not only is the leakage current of a FET a function of temperature, but so to a lesser extent are all the other parameters! Figure 15 illustrates the effect of temperature upon the transconductance curve, and it will be noticed that when V_{GS} is small, I_D has a negative temperature coefficient, which becomes positive when V_{GS} is large.

This change-over in sign is due to two different effects. Firstly, as the temperature increases the mobility of the charge carriers in the channel decreases, leading to an increasing channel resistance, and hence a fall in I_D . Secondly, the barrier potential of the junction has a negative temperature coefficient of about $-2.2\text{mV per }^{\circ}\text{C}$, which results in a rise of I_D with temperature.

At the point where these two effects cancel, the temperature coefficient of I_D becomes zero; this concept leads to a method of biasing the FET to have a very low drift performance⁷

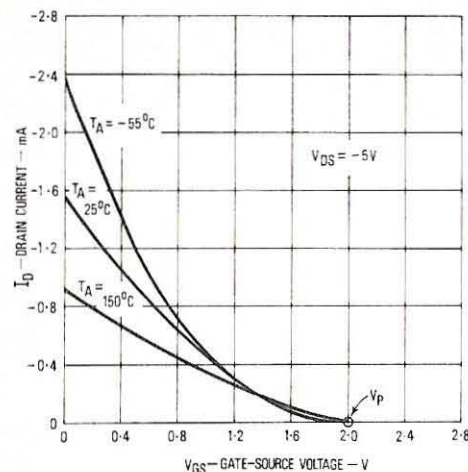


Figure 15. Effect of temperature on the transconductance curve of a typical P-channel FET.

Data sheets for FET's sometimes contain graphs or numerical values showing how the major parameters vary with temperature, so that account can be taken of such variations by the circuit designer.

The information so far presented is sufficient to establish bias design techniques but for purposes of small-signal handling — amplification, for example — the various capacitances associated with the FET structure must be considered, and an incremental equivalent circuit established.

2.4 Junction FET capacitances and the equivalent circuit

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometrical distribution are functions of the applied voltages V_{GS} and V_{DS} . Because of the complexity of dealing with such a distributed capacitance, the simplification is made that two lumped capacitances C_{gs} and C_{gd} exist between the gate and the source and drain respectively. (A much smaller capacitance C_{ds} also exists between the drain and the source, mainly due to the encapsulation components).

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be found) for specified operating conditions, and sometimes graphs are included which show their variation with V_{DS} , V_{GS} and temperature. Otherwise an estimate of inter-electrode capacitance values may be made by assuming that they vary inversely with the square root of the bias voltage; but that the temperature variations are very small because they depend upon the $-2.2\text{mV}/^\circ\text{C}$ change in junction potential difference.

Assuming that the FET is properly biased — that is, the d.c. conditions are met by the external circuitry — it becomes possible to construct an incremental equivalent circuit, or model, from which the small-signal or a.c. performance may be predicted. Such an equivalent circuit is shown in Figure 16, and has been built up as follows.

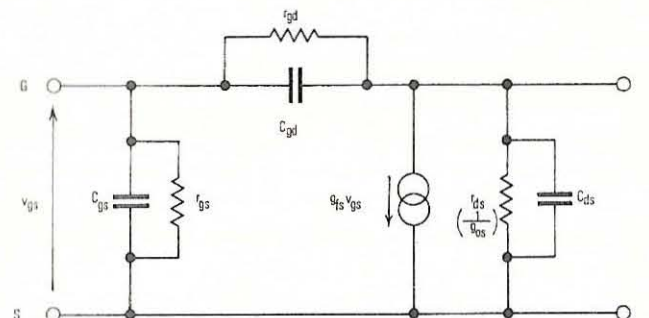


Figure 16. Incremental equivalent circuit for the junction FET.

Note: $C_{gss} = C_{iss} = C_{gs} + C_{gd}$

$C_{oss} = C_{gd} + C_{ds} \approx C_{gd} = C_{rss}$

(C_{ds} is largely the header capacitance and is therefore small enough to be ignored for most purposes).

The equivalent capacitance from the gate to the source, C_{gs} , is shunted by a very large input resistance r_{gs} , both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd} . (For most normal purposes r_{gs} and r_{gd} may be neglected and the gate impedance of the FET treated as purely capacitive). At the drain side of the equivalent circuit the small capacitance C_{ds} is shunted by the incremental channel resistance r_{ds} . This has been shown to be capable of wide variation, depending on bias conditions; but as the equivalent circuit is fundamentally relevant to the pinch-off, or saturated condition, r_{ds} will be of the order of megohms.

The incremental channel current is given by the transconductance g_{fs} multiplied by the incremental gate voltage; for the small signal, v_{gs} , this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET: that is, in the conventional 'positive' direction.

This completes a simple form of equivalent circuit for the junction FET, and makes possible the design of circuits around it. The actual values of g_{fs} and r_{ds} can be measured as previously mentioned, and it remains only to establish methods of determining C_{gs} and C_{gd} . (C_{ds} is much smaller than either and may be neglected).

Firstly, assume that the FET is in operation and that the drain is connected to the source, via a large capacitor :- that is, the drain and source are short-circuited to a.c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss} \text{ (or } C_{iss}) = C_{gs} + C_{gd} \quad \dots (2.5)$$

Secondly, assume that the gate and source are short-circuited to a.c. in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss} \text{ (or } C_{oss}) \approx C_{gd} \quad \dots (2.6)$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. Note that an alternative symbol for C_{gd} is C_{rss} , which refers to the 'reverse' capacitance.

In data sheets it is normal to quote $C_{gss} (=C_{iss})$ and $C_{dss} (=C_{oss})$. C_{rss} is often quoted in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usual, then $C_{rss} \approx C_{oss}$.

Should it be necessary to extract C_{gs} and C_{gd} , this can be done quite simply, using equations 2.5 and 2.6.

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \quad \dots (2.7)$$

and $C_{gd} = C_{rss} \quad \dots (2.8)$

(It should be remembered that all capacitance measurements should be made at the same bias levels since the capacitances are functions of applied voltages.)

To indicate the order of these capacitances, consider the data sheet for the Siliconix E102 N-channel FET. Here, they are given as,

$$C_{iss} \text{ (at } V_{DS} = 20V \text{ and } f = 1 \text{ MHz)} = 8pF \text{ (max)}$$

and

$$C_{rss} \text{ (at } V_{DS} = 20V \text{ and } f = 1 \text{ MHz)} = 3pF \text{ (max)}$$

Hence, at a drain-source voltage of 20V and at a frequency of 1 MHz $C_{gs} = 8 - 3 = 5pF$ maximum. Even though this FET is physically symmetrical, bias conditions have forced the capacitances C_{gs} and C_{gd} to be unequal.

2.5 Characteristics and parameters of the Insulated-Gate FET (MOSFET)

Chapter 1 indicated the primary difference between the insulated-gate and the junction FET; this being that the former has no gate-to-channel junction, but has instead a metallic gate insulated from the channel by a very thin layer of (usually) silicon-dioxide. This means that the gate voltage can be allowed to swing both positive and negative with respect to the channel, the result of which is best indicated by reference to Figure 17. The transconductance curves for the four types of MOSFET have been drawn in their correct quadrants, and related to their IEEE recommended symbols. Notice that, as

with junction FET's, all the transconductance curves are positive.

The two depletion type MOSFET's can operate in both depletion and enhancement modes; that is, the application of a gate voltage of one polarity will reduce I_D , while that of the opposite polarity will cause it to increase.⁵ Depletion type MOSFET's are called Type 'B' FET's according to JEDEC convention, and junction FET's are called Type 'A' FET's. Obviously the latter can only operate in the depletion region, otherwise the junctions would become forward-biased.

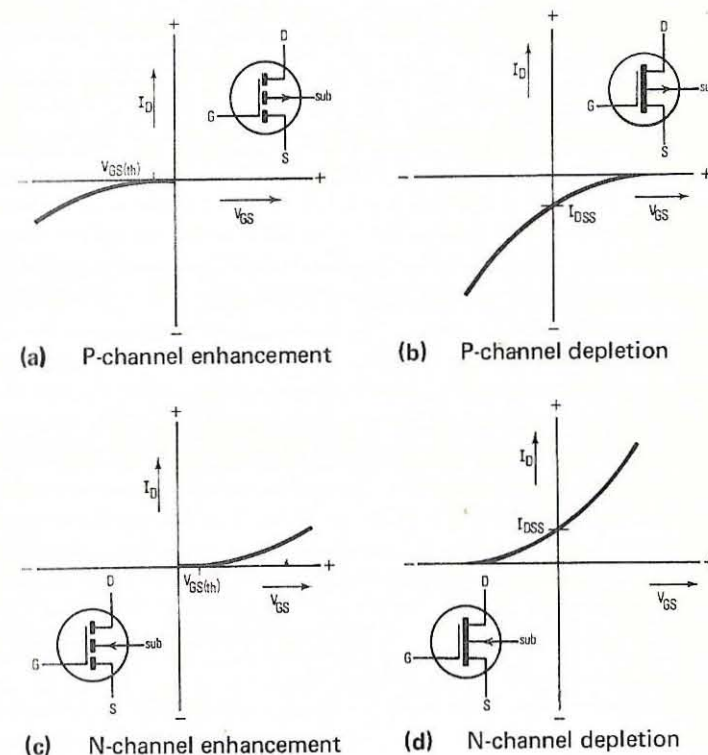


Figure 17. Symbols and transconductance curves for the family of insulated-gate FET's.

For a depletion MOSFET, the transconductance curve meets the y-axis at $I_D = I_{DSS}$, where $V_{GS} = 0$; just as does the transconductance curve for the junction FET. It must be remembered that I_D may be significantly increased over I_{DSS} by reversing the polarity of V_{GS} in the case of the depletion MOSFET. Sometimes a parameter $I_{D(ON)}$ is quoted at specified values of V_{GS} and V_{DS} as an indication of the ON performance of the device.

Actually, $I_{D(ON)}$ is a more appropriate parameter for the pure enhancement MOSFET's (or Type 'C' FETs), for, as can be seen from Figures 17 (a) and (c), their transconductance curves are shifted along the x-axis so far that I_{DSS} becomes very small indeed. In fact, for enhancement MOSFET's, I_{DSS} — consisting mainly of body-drain leakage — is quoted as a measure of the OFF performance of the device.

For example, in the case of the Siliconix M103 P-channel MOSFET:

$$I_{DSS} = -0.2\text{nA (max)} \text{ at } V_{DS} = -20\text{V}; V_{GS} = 0$$

The value of V_{GS} at which the channel just begins to conduct is called the **threshold voltage**, $V_{GS(th)}$, and for the M103 this is:

$$V_{GS(th)} = -3 \text{ to } -5\text{V at } I_D = 10\mu\text{A}; V_{GS} = V_{DS}; V_{BS} = 0$$

Here the phrase 'just begins to conduct' means $I_D = 10\mu\text{A}$, which is a common though somewhat arbitrary interpretation. (NOTE: Because the gate and drain voltages for an enhancement MOSFET are of the same polarity, it is reasonable to connect the gate to the drain for this measurement, giving $V_{GS} = V_{DS}$; and to connect the substrate or Body to the source, giving $V_{BS} = 0$).

The threshold voltage is analogous to V_p for junction FET's and is usually quoted only for enhancement MOSFET's. Depletion MOSFET's being normally-ON devices, need the application of a voltage to switch them OFF, and the value of V_{GS} which is guaranteed by the manufacturer to limit I_D to a very small value $I_{D(OFF)}$ is normally quoted.

At the end of Chapter 1 it was explained how the output characteristics bend over as $|V_{DS}|$ rises, and having now defined $V_{GS(th)}$, it can be seen that the locus separating the triode from the pentode regions must occur where $V_{DS} = V_{GS}$. That is:

$$|V_{DS}(\text{locus})| = |V_{GS}| - |V_{GS(th)}|$$

As was also explained in Chapter 1, P-channel enhancement and N-channel depletion MOSFET's are common, if only because the natural formation of an N-channel at an oxide-silicon interface makes manufacture of the alternative two types more difficult. But all four types do exist, and their transconductance curves, when working well into the saturation region, approximate to a square law of the form:

$$I_D = \frac{\beta}{2} [V_{GS} - V_{GS(th)}]^2 \quad \dots (2.9)$$

where β is the device constant and is a function of the geometry of the MOSFET:

$$\beta = \frac{\mu \epsilon_s W}{T_O L} \quad \dots (2.10)$$

where ϵ_s = dielectric constant
 μ = mobility (μ_n for electrons; μ_p for holes)
 L = channel length from source to drain
 W = channel width
 T_O = thickness of the gate insulation

The transconductance may be found by differentiating equation 2.9:

$$g_{fs} = \frac{dI_D}{dV_{GS}} = \beta [V_{GS} - V_{GS(th)}] \quad \dots (2.11)$$

Comparing equations 2.10 and 2.11 it can be seen that the value of g_{fs} is proportional to the channel dimensions for a given insulation thickness, i.e.:

$$g_{fs} \propto \frac{W}{L}$$

Unfortunately, increasing the channel width to make g_{fs} large also increases the gate-channel capacitance — and the length can obviously not be reduced below a certain practical minimum. This situation epitomises the sort of compromise which must always be made in the design of transistor devices.

Output characteristics for N-channel depletion and P-channel enhancement MOSFET's appeared in Figures 7 and 8. From them the incremental channel resistance will be seen to vary in much the same manner as for the junction FET, which means that the MOSFET can also be used as a voltage-controlled resistor, or as a low-level switch when operated below pinch-off.

The situation regarding breakdown voltages is quite unique, however. Because the gate-channel insulation presents an extremely high resistance — up to 10^{16} ohms in fact — but is very thin, it is subject to catastrophic breakdown by overvoltages. For example, the small gate-channel capacitance can easily be charged up to hundreds or even thousands of volts in a dry climate merely by the friction involved in extracting the MOSFET from its package, and this is more than enough to punch a minute hole through the silicon dioxide — so destroying the device even before use!

For this reason many MOSFET's (including the Siliconix M103) contain internal protective Zener diodes between gate and source. This technique, however, lowers the gate-channel resistance, and I_{GSS} rises to levels typical of junction FET's — which may be undesirable if the MOSFET is to be used as the input stage of an electrometer amplifier, for example. An alternative form of protection is to short-circuit all the leads until the device has been soldered into place, and this is normally accomplished by a shorting clip fitted by the manufacturer prior to despatch.

In the absence of a Zener diode the breakdown voltage of the insulating layer determines those maximum allowable applied voltages which actually appear across this layer. These include BV_{GSS} , BV_{GDO} and BV_{GSO} . Recalling that in

the MOSFET source-substrate and drain-substrate PN junctions exist, than a further maximum allowed voltage must be specified to take these into account. For the enhancement (normally-OFF) MOSFET this is BV_{DSS} at $V_{BS} = 0$; that is, the drain to source voltage when both gate and substrate (body) are connected to the source. For the depletion MOSFET this parameter would be BV_{DSX} at $V_{BS} = 0$, for to reduce I_D to zero a specified gate voltage would have to be applied. Because of the existence of two distinct breakdown mechanisms, both BV_G and BV_D parameters are provided in the relevant data sheets.

The capacitances associated with MOSFET's can be lumped, and referred to an approximate equivalent circuit as can those for the junction FET. A crude equivalent circuit would be similar to that of Figure 16 with the deletion of r_{gd} and r_{gs} plus the addition of a pair of diodes connected from the substrate to the source and drain respectively. The polarity of the diodes would depend upon whether the MOSFET in question were N or P-channel. Discrete MOSFET's are not commonly employed in low frequency linear amplification applications (except where an extraordinarily high input resistance is demanded) because they exhibit much higher noise figures than junction types. Hence equivalent circuits of the form of Figure 16 are not particularly useful.

2.6 Summary

The leading parameters and characteristics relevant to all six of the family of field effect transistors having been presented, they can now be used to establish both biasing and small-signal design techniques. Where new parameters are required — such as the matching parameters for dual FET's — they will be introduced in the appropriate sections.

Chapter 3

BIASING AND AUDIO-FREQUENCY AMPLIFICATION

3.1 Introduction

The field effect transistor being fundamentally a three-terminal device, there are three ways in which it may be connected to form a linear amplifier stage. In two of them, the common-source (CS) and common-drain (CD) configurations, the gate is used as the input terminal — which means that at the lower frequencies it is possible to exploit the extremely high input resistance presented. As the frequency increases, however, the input capacitance becomes dominant, and the input reactance becomes progressively smaller. This is particularly so for the CS stage, due to the Miller effect described later. But the Miller Effect is very small in the common-gate (CG) stage, so this configuration can be used for high-frequency work. The input terminal is the source under these conditions, so a lower input impedance than would be the case for gate input is presented.

Before the FET can be used to amplify small signals it must be biased to some suitable operating point by circuitry which will achieve the desired result irrespective of parameter spreads. That is to say, any FET of the chosen type number must work in the circuit; and further, it must do so over the full temperature range which the circuit is liable to experience. It is therefore logical to consider bias design first.

3.2 Biasing Circuit Design

The most useful characteristic of a small-signal FET in bias design is the transconductance curve, as its position is fully defined by the data sheet values of I_{DSS} and V_p — modified if necessary for the temperature range chosen. 'Maximum' and 'minimum' transconductance curves for a particular FET (the Siliconix E102) were given in Figure 10, page 20, but in the interests of a general design procedure encompassing both N and P-channel FET's, a similar pair of curves is drawn in the first quadrant in Figure 18.

Consider the simple biasing circuit of Figure 19. Here the quiescent, or d.c. channel current, I_Q , passes through the source resistor R_S to produce a voltage drop $I_Q R_S$. The two resistors R_1 and R_2 hold the gate at a fixed voltage V_B with respect to the common line. Summing voltages around the gate-source- R_2 loop gives:

$$V_{GSQ} = I_Q R_S - V_B \quad \dots (3.1)$$

This is the equation to a straight line whose slope is R_S and whose intercept with the axis is $-V_B$. This is called the **bias line**, and its intersection with the limiting transconductance curves will give the 'maximum' and 'minimum' operating, or

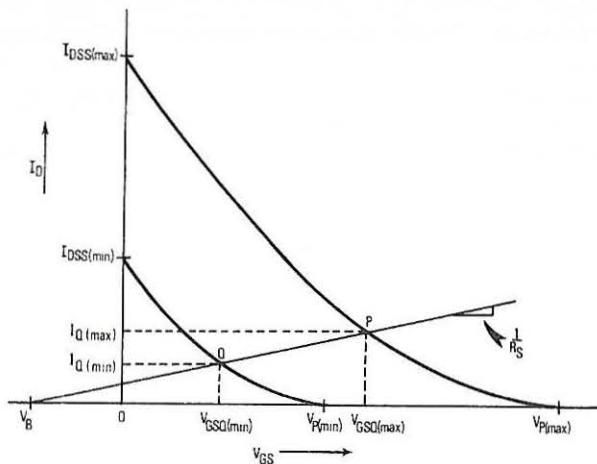


Figure 18. *The bias-line.*

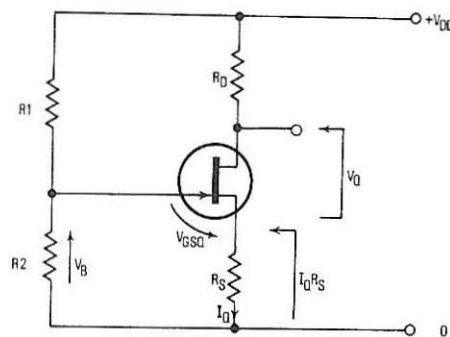


Figure 19. *Simple biasing circuit.*

quiescent working points P and Q – as shown in Figure 18.

The change in I_Q from the maximum to the minimum unit, ΔI_Q , is simply $I_{Q(max)} - I_{Q(min)}$; which means that the corresponding change in drain voltage is $R_D \Delta I_Q$. This is usually an important design parameter, as an excessive voltage swing in either direction could lead to clipping of the signal waveform.

Similarly the maximum change in quiescent gate-source voltage is $\Delta V_{GSQ} = V_{GSQ(max)} - V_{GSQ(min)}$.

From the geometry of Figure 18 the values of both R_S and V_B may be determined:⁶

$$R_S = \frac{\Delta V_{GSQ}}{\Delta I_Q} \quad \dots (3.2)$$

and

$$V_B = \frac{V_{GSQ(min)} I_{Q(max)} - V_{GSQ(max)} I_{Q(min)}}{\Delta I_Q} \quad \dots (3.3)$$

which is a standard geometrical expression.

Because the limits of I_Q are usually known (being design parameters), it remains only to find the limits of V_{GSQ} before equations 3.2 and 3.3 can be used. These may be determined simply by re-writing equation 2.1 in the form:

$$V_{GSQ(min)} = V_{P(min)} \left[1 - \sqrt{\frac{I_{Q(min)}}{I_{DSS(min)}}} \right] \quad \dots (3.4a)$$

and

$$V_{GSQ(max)} = V_{P(max)} \left[1 - \sqrt{\frac{I_{Q(max)}}{I_{DSS(max)}}} \right] \quad \dots (3.4b)$$

A design example

Suppose that a Siliconix E102 N-channel FET is to be used in the circuit of Figure 19 along with an 18V power supply; and that the maximum permissible variation in the quiescent source-drain voltage, ΔV_Q , is 2V centred around a nominal drain voltage of 14V with respect to the common line.

Because $I_{DSS(min)} = 0.9$ mA for the E102, a reasonable value for I_Q would be 0.5 mA.

$$\text{Hence } R_D = \frac{V_{RD}}{I_{Q(nom)}} = \frac{18 - 14}{0.5} = 8 \text{ kilohms (or 8.2 kilohms to the nearest preferred value)}$$

$$\text{This leads to } \Delta I_Q = \frac{\Delta V_Q}{R_D} = \frac{2}{8.2} = 0.24 \text{ mA}$$

so that I_Q may vary between:

$$I_{Q(max)} = 0.5 + \frac{0.24}{2} = 0.62 \text{ mA}$$

$$\text{and } I_{Q(min)} = 0.5 - \frac{0.24}{2} = 0.38 \text{ mA}$$

Using equations 3.4 and the data sheet values of V_p :

$$V_{GSQ(min)} = 0.8 \left[1 - \sqrt{\frac{0.38}{0.9}} \right] = 0.28V$$

$$V_{GSQ(max)} = 4.0 \left[1 - \sqrt{\frac{0.62}{4.5}} \right] = 2.51V$$

giving $\Delta V_{GSQ} = 2.51 - 0.28 = 2.23V$

Equations 3.2 and 3.3 now give

$$R_S = \frac{\Delta V_{GSQ}}{\Delta I_Q} = \frac{2.23}{0.24} = 9.1 \text{ kilohms}$$

and

$$V_B = \frac{(0.28 \times 0.62) - (2.51 \times 0.38)}{0.24} = -3.25V$$

To obtain a bias voltage of 3.25V, R_1 may conveniently be 150 kilohms and R_2 may be 33 kilohms or any other values in the same ratio.

3.3 Tolerances in bias design

The two transconductance curves of Figure 18 have taken into account unit-to-unit tolerances. In order that they should also cope with temperature variations, the limiting values of I_{DSS} and V_p should be modified according to data sheet information.

The resistors involved are also subject to unit-to-unit tolerances, and to temperature variations. If minimum and maximum values are assigned to R_S , then the slope of the bias line changes; and the tolerance ranges of R_1 and R_2 will cause V_B to shift along the x-axis from a point corresponding to

$$V_{B(min)} = \frac{V_{DD} \cdot R_2(min)}{R_1(max) + R_2(max)} \quad \dots (3.5a)$$

to

$$V_{B(max)} = \frac{V_{DD} \cdot R_2(max)}{R_1(min) + R_2(min)} \quad \dots (3.5b)$$

The overall result is that there will be an area on the transconductance graph which contains all the possible operating points of the FET in question. This situation is illustrated in Figure 20.

3.4 Bias stability

The biasing network of Figure 19 is only one of many possible circuits, but it is one of the most common. Its efficiency in stabilizing the working point against both unit-to-unit changes and against temperature variations is implicit in the operating area diagram of Figure 20. A figure of merit showing by how much

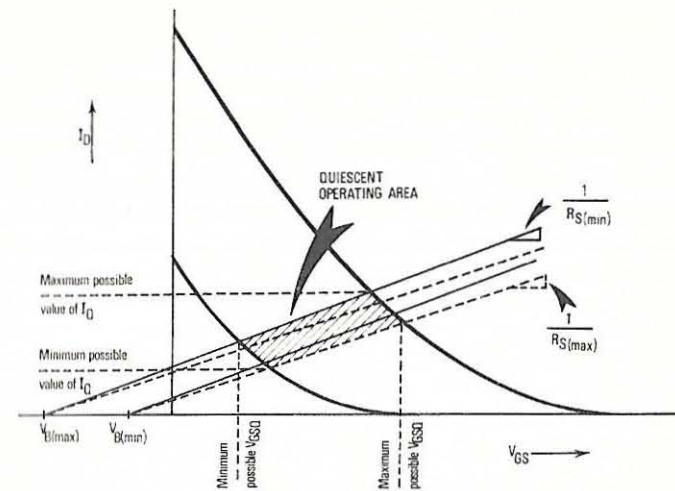


Figure 20. The quiescent operating area.

the change in I_Q has been reduced below that for an unstabilized stage may be determined as follows:

I_Q is a function of both temperature T and V_{GSQ} . That is

$$I_Q = f(T, V_{GSQ})$$

Over a temperature range δT , I_Q will change by δI_Q :

$$\begin{aligned} \delta I_Q &= \frac{\partial I_Q}{\partial T} \delta T + \frac{\partial I_Q}{\partial V_{GSQ}} \delta V_{GSQ} \\ &= \frac{\partial I_Q}{\partial T} \delta T - g_{fs} \delta I_Q R_S \end{aligned}$$

$$\text{giving} \quad \delta I_Q (1 + g_{fs} R_S) = \frac{\partial I_Q}{\partial T} \delta T$$

Now $\frac{\partial I_Q}{\partial T} \delta T = \delta I_{Q(0)}$, which is the drift in I_Q when $R_S = 0$; that is, when no bias stabilization takes place. Hence a figure of merit (or **stability factor**) can be defined:

$$SF = \frac{\text{Drift in } I_Q \text{ with } R_S}{\text{Drift in } I_Q \text{ without } R_S} = \frac{\delta I_Q}{\delta I_{Q(0)}} = \frac{1}{1 + g_{fs} R_S} \quad \dots (3.6)$$

Notice that as this is a case of an internal change being reduced by the application of negative feedback, then $(1 + g_{fs} R_S)$ must be the **feedback factor** for the circuit – a concept which is often useful in small-signal work.

3.5 The common-source stage

Whereas only biasing components were shown in Figure 19, the circuit in Figure 21 (a) represents a complete CS small-signal amplifier stage. It has been assumed that the signal-source may contain a d.c. path and the coupling capacitor C_C exists to prevent the shunting of R_2 , which would otherwise change the value of V_B . Also a decoupling capacitor C_S is included to short-circuit R_S to a.c. at the signal frequencies of interest.

Notice that, to the right of C_C , the input resistance 'seen' by the signal is the parallel combination $R_1//R_2$, which is much smaller than r_{gs} or r_{gd} . If it is desired to exploit the inherent high input resistance properties of the FET, R_1 and R_2 can be made small and a high value series gate resistor R_3 included — as shown in Figure 21 (b). This, incidentally, makes possible a more accurate definition of V_B since closer tolerances are more readily available for lower value resistances. The input resistance to the right of C_C is now essentially R_3 (which is still much less than r_{gs} or r_{gd}).

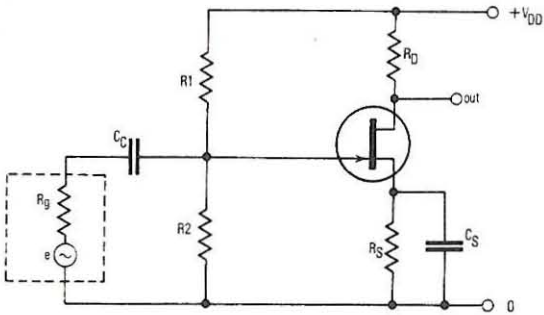


Figure 21a Simple CS circuit

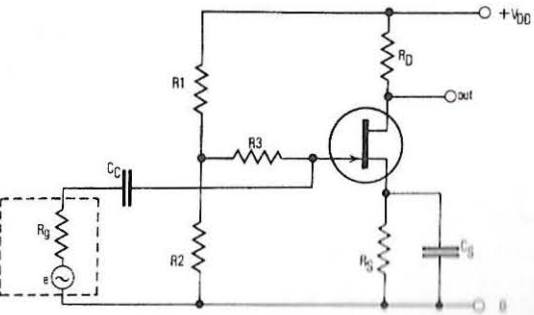


Figure 21b CS circuit modified for low R_1 and R_2 and high R_3 .

Unfortunately, if R_3 is made extremely large, the voltage-drop $I_G.R_3$ (where I_G is the gate current under the relevant operating conditions), will change the bias — being additive with V_B . Although this can be an embarrassment (I_G being a marked function of temperature), it may be taken into account in the bias design by replacing the limits of V_B with those of $V_B + I_G.R_3$

Figure 22 (a) gives the complete equivalent circuit for the stage, but certain simplifications can be made for the purposes of gain and impedance calculations. Initially these calculations will be made with reference to the right of the points a b; that is, looking into the FET itself. In all cases r_{gs} and r_{gd} are omitted, being very large.

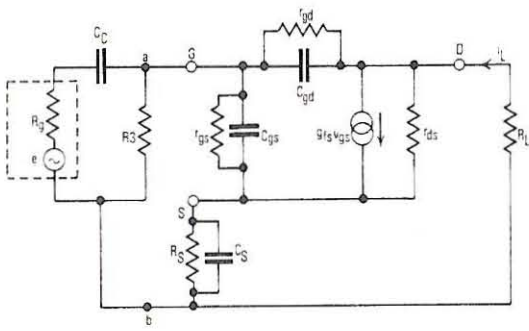
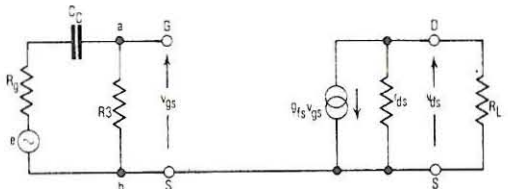
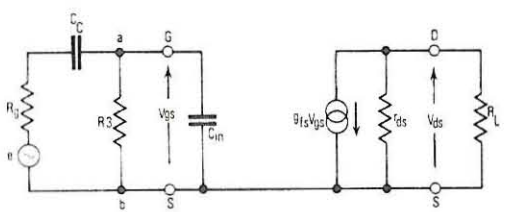


Figure 22 (a) Complete equivalent circuit for CS stage.



(b) L.F. equivalent circuit simplification.



(c) H.F. equivalent circuit simplification ($C_{in} = C_{iss} - A_v C_{rss}$).

- (i) At low frequencies, where C_{gs} and C_{gd} are unimportant, but where X_{CS} is still small enough to effectively short-circuit R_S , the simplification provided in Figure 22 (b) is valid. (It is also valid for biasing schemes where R_S is zero). If R_L is the combination of R_D and any external load, then the voltage gain is:

$$A_{V(l.f.)} = \frac{v_{out}}{v_{in}} = \frac{v_{ds}}{v_{gs}} = \frac{-g_{fs}v_{gs}}{v_{gs}} \left(\frac{r_{ds}R_L}{r_{ds} + R_L} \right)$$

and if $r_{ds} \gg R_L$, which is usual, this becomes:

$$A_{V(l.f.)} \approx -g_{fs}R_L \quad \dots (3.7)$$

The input resistance is, of course, just R_3 .

- (ii) At higher frequencies, the Miller Effect comes into play, because C_{gd} appears across the amplifier; thus its capacitance is increased to $C_{gd}(1 - A_V)$. This well-known effect is demonstrated in Figure 23, which is self-explanatory.

The total input capacitance is now:

$$C_{in} = C_{gs} + C_{gd}(1 - A_V) \quad \dots (3.8a)$$

or

$$\begin{aligned} C_{in} &= (C_{iss} - C_{rss}) + C_{rss}(1 - A_V) \\ &= C_{iss} - A_V \cdot C_{rss} \end{aligned} \quad \dots (3.8b)$$

The equivalent circuit is now as shown in Figure 22 (c). Note that V_{gs} and V_{gd} refer to small signals which must by definition be sinusoidal because reactance calculations are involved.

The calculation of voltage gain for the circuit is now somewhat more complicated, but may be shown to be:

$$A_V = A_{V(l.f.)} \left[\frac{\frac{g_{fs}}{X_{C_{gd}}} - 1}{\frac{g_{fs}}{X_{C_{gd}}} - A_{V(l.f.)}} \right] \quad \dots (3.9)$$

and the input impedance is simply the reactance $X_{C_{in}} // R_3$.

6 Frequency response of the CS stage

Referring to Figure 22 (c), if $C_C \gg C_{in}$ (which is usual), then the high frequency cut-off point f_H , at which V_{gs} (and hence V_{ds}) is 3 dB below its maximum value occurs when:

$$R_g // R_3 = |X_{C_{in}}|$$

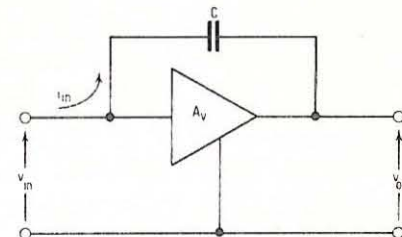
that is

$$f_H = \frac{R_g + R_3}{2\pi R_g R_3 C_{in}} \quad \dots (3.10)$$

This argument will be clearly seen if the Norton form of the generator is drawn, when R_g is obviously in parallel with R_3 , and both in parallel with C_{in} .

Figure 23. Demonstration of the

$$\begin{aligned} v_{in} - v_{out} &= \frac{1}{C} \int i_{in} dt \\ \text{or } v_{in}(1 - A_V) &= \frac{1}{C} \int i_{in} dt \\ \text{or } v_{in} &= \frac{1}{C(1 - A_V)} \int i_{in} dt \\ \text{which shows that} \\ C_{in} &= C(1 - A_V). \end{aligned}$$



The low-frequency cut-off point f_L is affected by two parts of the CS circuit. Referring to Figure 22 (a);

If $|X_{CS}|$ is much less than the resistance at the source terminal, that is,

$$\text{if } |X_{CS}| \ll \frac{1}{g_{fs}} \quad (\text{as will be shown later}),$$

then near the low frequency cut-off point

$$f_L \text{ occurs when } |X_{C_C}| = (R_g + R_3)$$

That is:

$$f_L = \frac{1}{2\pi (R_g + R_3) C_C} \quad \dots (3.11a)$$

If $|X_{C_C}| \ll (R_g + R_3)$ near the low frequency cut-off point,

then f_L occurs when $|X_{C_S}| = R^I$.

Here R^I is the parallel combination of R_S and the output resistance of the stage at the source terminal. This latter resistance can be shown to be approx.

$$\frac{1}{g_{fs}}, \text{ so that: } f_L = \frac{1}{2\pi R^I C_S} \quad \dots (3.11b)$$

where

$$R^I = \frac{R_S/g_{fs}}{R_S + 1/g_{fs}} = \frac{R_S}{1 + R_S g_{fs}} \quad \dots (3.11c)$$

If the input and source time-constants are similar, both will affect the position of f_L , and the low-frequency roll-off will tend to 12 dB per octave rather than the 6 dB per octave which is characteristic of a single time-constant slope.

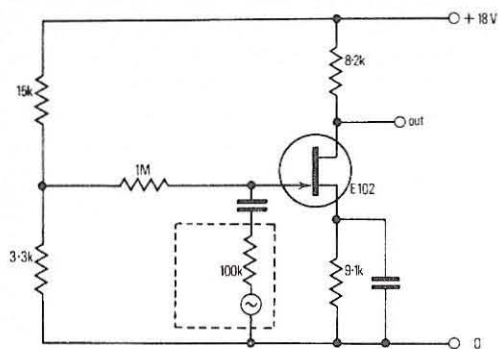


Figure 24. Practical CS stage showing 100k Ω signal-source in use.

A design example (continued)

Figure 24 shows the circuit of a CS stage based on the bias design carried out in Section 3.2. Using equation 3.7, the small-signal voltage gain may be determined:

$$A_{v(l.f.)} \simeq g_{fs} R_L = -10^{-3} \times 8.2 \times 10^3 = -8.2$$

To obtain a quick approximate solution g_{fs} has been interpreted as $g_{fs0(min)}$. Strictly speaking, gain limits should have been calculated by first obtaining $g_{fs(max)}$ and $g_{fs(min)}$ from equation 2.4, page 18, using the previously calculated values of $V_{GSQ(min)}$ and $V_{GSQ(max)}$. This quick calculation does, however, give the approximate gain to be expected, and an actual circuit using an arbitrary E102 exhibited a gain of -8.5 .

From the data sheet 'maximum' values of C_{iss} and C_{rss} may be inserted into * equations 3.8b, giving the 'worst case' value of C_{in} :

$$C_{in} = C_{iss} - A_v C_{rss} = 8 + (8.2 \times 3) = 32.6 \text{ pF}$$

This value may be inserted into equation 3.4 to give the lowest value expected for the high-frequency cut-off point:

$$f_H(min) = \frac{R_g + R_3}{2\pi R_g R_3 C_{in}} = \frac{(10^5 + 10^6) 10^{12}}{2\pi (10^5 \times 10^6) 32.6} = 53.7 \text{ kHz}$$

(a measured value of f_H was 72 kHz)

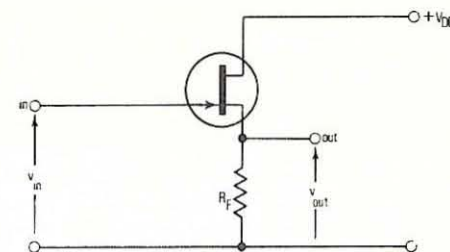
Using a values of C_C and C_S shown, f_L is less than 10 Hz.

3.7 The source-follower (or CD) stage

Figure 25 shows the CD configuration, less the gate bias components. These will be similar to those for the CS mode. The source resistor is now unbypassed, meaning that degeneration or series-signal feedback occurs.

*NOTE: Capacitance values can exceed Data Sheet maxima under different bias conditions from those specified, being inversely proportional to the d.c. bias voltage.

Figure 25. The source-follower (CD) stage.



The voltage gain may be found very simply for low frequencies:

$$A_{v(l.f.)} = \frac{v_{out}}{v_{in}} = \frac{i_d R_F}{v_{gs} + i_d R_F} = \frac{g_{fs} v_{gs} R_F}{v_{gs} + g_{fs} v_{gs} R_F} = \frac{g_{fs} R_F}{1 + g_{fs} R_F} \quad \dots (3.12)$$

Notice that there is no phase reversal implied by this expression; and that if $g_{fs} R_F \gg 1$, it approximates to unity gain.

The input impedance of the CD stage will remain large at much higher frequencies than for the CS stage because the input capacitance is not augmented by the Miller Effect. A simple analysis of the equivalent circuit will show that:

$$C_{in} = C_{gd} + C_{gs} (1 - A_v) = C_{rss} A_v + C_{iss} (1 - A_v)$$

which is very small because A_v is positive and slightly less than unity.

The analysis also shows that the output conductance at low frequencies is:

$$G_{out} = \frac{1}{R_F} + \frac{1}{r_{ds}} + g_{fs}$$

which for normal numerical values reduces to:

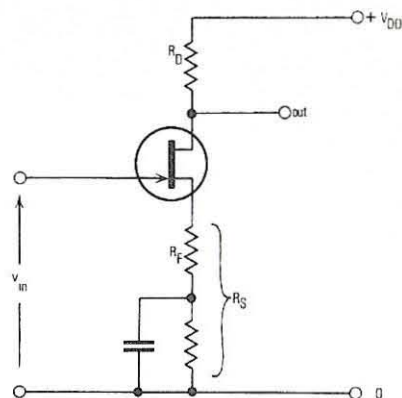
$$G_{out} \simeq g_{fs}; \quad \text{or } R_{out} \simeq \frac{1}{g_{fs}} \quad \dots (3.13)$$

Because this can be quite a low value, the CD stage may be used as a highly effective impedance changer, or buffer stage. It should be borne in mind however, that an offset voltage V_{GS} exists between input and output, so that in cases where a d.c. buffer with equal input and output potentials is required, it will also be necessary to incorporate a level-shifting stage.

3.8 The Degenerate CS stage

In Figure 26 part of the source resistor R_S has been left unbypassed, which means that the stage will behave in part like a CS stage with an output signal appearing at the drain; and in part like a CD stage, with an output appearing at the source.

Figure 26. *The degenerate CS stage.*



From gate to drain the voltage gain is:

$$A_v(\text{CS}) = \frac{-i_d R_D}{v_{in}} = \frac{-i_d R_D R_F}{v_{in} R_F} \quad \dots (3.14)$$

Now the signal developed across R_F is $i_d R_F$, which is by definition the input signal multiplied by the CD voltage gain. Using equation 3.12 this is:

$$i_d R_F = \frac{v_{in} g_{fs} R_F}{1 + g_{fs} R_F} \quad \dots (3.15)$$

This expression may be inserted into equation 3.14 to give:

$$A_v(\text{CS}) = \frac{-g_{fs} R_D}{1 + g_{fs} R_F} \quad \dots (3.16)$$

If $g_{fs} R_F \gg 1$ (which is not necessarily true):

$$A_v(\text{CS}) \simeq -\frac{R_D}{R_F}$$

Note the resemblance between equations 3.16 and 3.6. This is because in both cases the denominator is the feedback factor for the circuit. If ALL of R_S is left unbypassed, then $R_F = R_S$ and the a.c. feedback factor is the same as the d.c. feedback factor.

The degenerate CS stage provides a more stable, albeit lower gain, than does the simple CS stage, particularly when g_{fs} is sufficiently high to allow equation 3.16 to reduce to $-R_D/R_F$. It is also useful as a phase-splitting stage, for if $R_F = R_D$,

outputs equal in magnitude and opposite in phase will appear at the source and drain respectively.

3.9 Bootstrapping

An extremely useful self-biasing modification of the source-follower is shown in Figure 27. This is a 'bootstrapped' circuit, wherein positive feedback is applied to R_3 — so increasing its apparent value. The bias voltage for the stage is provided by the voltage drop across R_{F1} . That is:

$$V_{GSQ} = I_Q R_{F1}$$

which can be inserted into equation 2.1, page 18, to give:

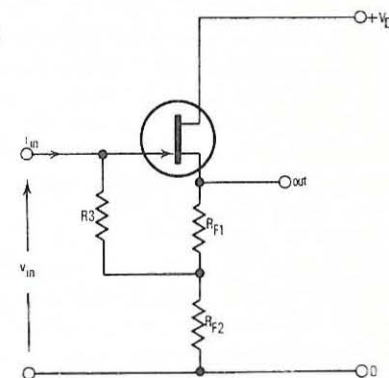
$$I_Q = I_{DSS} \left[1 - \frac{I_Q R_{F1}}{V_P} \right]^2$$

The value of R_{F1} which will result in the required value of I_Q may be extracted from this equation:

$$R_{F1} = \frac{V_P}{I_Q} \left[1 - \sqrt{\frac{I_Q}{I_{DSS}}} \right]$$

Clearly the limits of V_P and I_{DSS} may be easily inserted to give a fully tolerated bias design.

Figure 27. *The bootstrap follower.*



The input resistance may be found by writing a simple expression for the small-signal input current:

$$i_{in} = \frac{v_{in} - i_d R_{F2}}{R_3} = \frac{v_{in} - g_{fs} v_{gs} R_{F2}}{R_3}$$

and inserting an equally obvious expression for v_{gs} :

$$v_{gs} = v_{in} - i_d (R_{F1} + R_{F2}) = v_{in} - g_{fs} v_{gs} (R_{F1} + R_{F2})$$

After a little manipulation this leads to:

$$R_{in} = R_3 \left[\frac{1 + g_{fs}(R_{F1} + R_{F2})}{1 + g_{fs}R_{F1}} \right]$$

Notice that if $R_{F2} = 0$ (that is, R_3 goes to ground), $R_{in} = R_3$; and if $R_{F1} = 0$ (that is, R_3 goes to the source terminal),

$$R_{in} = R_3 (1 + g_{fs}R_{F2}) = \frac{R_3}{1 - A_v(CD)} \text{ because from equation 3.12:}$$

$$A_v(CD) = \frac{g_{fs}R_F}{1 + g_{fs}R_F}$$

and in this case $R_F = R_{F2}$. Note that this connection is impossible for obvious biasing reasons; if an alternative bias system is used, however, a bootstrapping capacitor may be connected to the source.

3.10 Choice of operating point

The nominal position chosen for the operating or quiescent point on the transconductance curve depends upon the specification for which the amplifier stage is to be designed. As has already been pointed out, the amplitude of the output signal will determine the quiescent voltage appearing at the output point — that is, the drain in the case of the CS stage. Knowing the power supply voltage, and the maximum quiescent voltages which can appear across the resistor and channel respectively, it is easy to determine the nominal voltage drop across R_D , and also the amount by which it may be allowed to vary. This drop, V_{RD} , being usually defined by the specifications for the stage, may be treated thereafter as a constant; and the next design problem becomes the determination of I_Q . Clearly, for constant V_{RD} ($= I_Q R_D$), I_Q will vary inversely with R_D .

If low distortion is required, it is logical to operate on the least curved part of the transconductance curve; that is, where I_Q approaches I_{DSS} . Care must be taken

to ensure that neither temperature variations in I_Q , nor signal excursions, can take the operating point too close to I_{DSS} , or signal clipping will occur.

Conversely, if a high voltage gain is required and distortion is not of prime interest then the operating point should be moved down the curve to the region where V_{GS} approaches V_p , as shown in Figure 28. That operation in this region should result in high voltage gain is not obvious at first sight, for the value of g_{fs} is low, and rises to a maximum g_{fso} , at $I_Q = I_{DSS}$. If equation 3.7, page 40, is examined (i.e. $A_v \approx -g_{fs}R_D$), it is clear that A_v varies with both g_{fs} and R_D . Now R_D is an inverse function of I_Q (that is, $R_D = V_{RD}/I_Q$); whereas g_{fs} is given by equation 2.2, page 18. Putting these facts together, the voltage gain can be written:

$$A_v \approx -g_{fs}R_D = \frac{-g_{fs}V_{RD}}{I_Q} \approx \frac{-\frac{2I_{DSS}}{V_p} \left[1 - \frac{V_{GSQ}}{V_p} \right] V_{RD}}{I_{DSS} \left[1 - \frac{V_{GSQ}}{V_p} \right]^2}$$

or

$$A_v \approx \frac{-2V_{RD}}{V_p - V_{GSQ}} \quad \dots (3.17)$$

Although this equation, being an approximation, breaks down when $V_{GSQ} \rightarrow V_p$, it nevertheless indicates that maximal voltage gain occurs in this region. It also shows that at the opposite extreme, where $V_{GSQ} \rightarrow 0$, the minimal voltage gain is given by:

$$A_v(\min) = -\frac{2V_{RD}}{V_p} \quad \dots (3.18)$$

Between the two extremes — representing low distortion and high gain conditions — lies the minimal d.c. (or I_D) drift point. Here the transconductance curves for different temperatures coalesce. Unfortunately they do not meet at a single point, otherwise a bias line passing through that point would represent a condition of zero I_D drift. It is possible to achieve minimal drift by biasing in this region, but as each FET has a unique set of transconductance characteristics, individual adjustment must be made to the circuitry relevant to each unit.

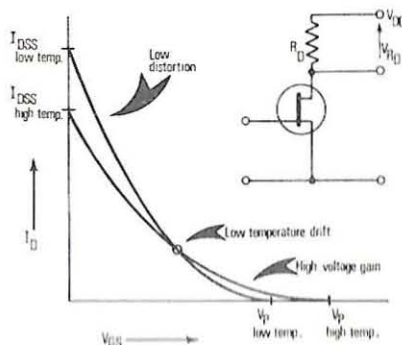
If V_p and I_{DSS} are known for a given unit, then the approximate position of the operating point may be calculated from:⁷

$$|V_{GSQ}(Z)| \approx |V_p| - K \quad \dots (3.19)$$

K being approximately
0.63 for P-channel
0.9 for N-channel

Where individual trimming of R_S is acceptable, it is quite possible to achieve voltage drifts at the output of a source-follower of less than $100\mu V$ over the

Figure 28. Operating regions on the transconductance curves for constant V_{RD} (or $I_Q R_D$).



temperature range 0 - 100°C. This procedure is, however, seldom suitable for production purposes.

Much improved drift figures may be obtained by the use of matched pairs of FET's, and these will be considered in Chapter 4, Section 4.5.

Having determined the general operating region for a device in the light of design specifications, it may be useful to know by how much the signal will be distorted during its passage through the stage: and also how much noise is likely to be added.

3.11 Distortion

As the transconductance curve approximates to a square-law, any incoming sinusoidal signal will give rise to harmonics. For a perfect square-law the highest harmonic would be the second, but for a real FET higher but much smaller harmonics will also exist. To determine the magnitude of the zero frequency, fundamental and second harmonics, however, it is necessary only to use the square-law and insert the total value of the input voltage and the output current:

$$i_D = I_{DSS} \left[1 - \frac{v_{GS}}{V_P} \right]^2 \quad \dots (3.20)$$

Here the quiescent value plus a single sinusoidal signal may be combined so that:

$$v_{GS} = V_{GSQ} + V_{\sin \omega t}$$

By inserting this expression into equation 3.20, expanding, and extracting the various components, it may be shown that the harmonic distortion factor D_H , defined as follows, is:⁸

$$\frac{\text{r.m.s. value of second harmonic}}{\text{r.m.s. value of fundamental}} = D_H = \frac{V}{4(V_{GSQ} - V_P)}$$

$$\text{where } V \text{ is the peak amplitude of the signal} \quad \dots (3.21)$$

Notice that this equation confirms the common-sense observation of Section 3.10 – that for minimum distortion V_{GSQ} should approach zero. It also shows that distortion increases with signal amplitude, which is reasonable, because a large signal will obviously cause working point excursions over more of the transconductance curve than will a small signal.

In general the amplification of a single frequency is a rare requirement; the input signal more often consists of a complex waveform. This means that intermodulation distortion will also occur, and this can be most easily demonstrated by postulating that two sinusoids are to be concurrently amplified.

That is

$$v_{GS} = V_{GSQ} + V_A \sin \omega_A t + V_B \sin \omega_B t$$

The output current will contain both sum and difference components of the two

sinusoids, and an intermodulation distortion factor D_I may be defined, and its value extracted:

$$\begin{aligned} \frac{\text{r.m.s. value of intermodulation components}}{\text{r.m.s. value of fundamental}} &= D_I \\ &= \frac{V_A V_B}{\sqrt{2}(V_{GSQ} - V_P)(V_A^2 + V_B^2)^{1/2}} \quad \dots (3.22) \end{aligned}$$

Here again the distortion is seen to be minimized by biasing near $V_{GSQ} = 0$.

The curvature of the transconductance characteristic is not the only cause of distortion,⁸ though it is the most important. Also involved are changes in the output conductance g_{OS} with working point, and with V_{DS} . However, to some extent changes in g_{fs} and g_{OS} work in opposition, and there is in fact a minimum distortion region defined from this point of view.

As the application of feedback to a stage reduces internally generated distortion, both D_H and D_I should be susceptible to improvement. This is in fact so, and in the general case they are divided by the value of the feedback factor for any given circuit. For example, in the simple case of series feedback, where a part R_F of the source resistor is left unbypassed (Figure 26), the two factors become:

$$D_H = \frac{V}{4(V_{GSQ} - V_P)(1 + g_{fs} R_F)}$$

and

$$D_I = \frac{V_A V_B}{\sqrt{2}(V_{GSQ} - V_P)(V_A^2 + V_B^2)^{1/2}(1 + g_{fs} R_F)}$$

In general feedback reduces not only the harmonic and intermodulation distortion, but also the internally generated noise (see the next Section). But the gain of the system is also reduced by the same amount, though the bandwidth is increased. This means that a given amplifier is not improved overall by the employment of feedback, but that if a much higher-gain amplifier is designed, and the gain is then reduced by the addition of feedback, this will constitute a system which exhibits lower distortion and noise than would an amplifier designed for the required gain without feedback.

3.12 Noise in FET stages

When a signal is applied to the input of an amplifier, it is inevitably accompanied by some noise, the amount of which is defined by the input signal-to-noise ratio. After amplification, the signal will be associated with a larger proportion of noise – contributed by noisy elements within the amplifier itself. Thus the output signal/noise ratio will be smaller than the input S/N ratio. The two ratios may be compared to define a noise factor, NF:

$$NF = \frac{\text{Input signal power/input noise power}}{\text{Output signal power/output noise power}} = \frac{PS(in)/PN(in)}{PS(out)/PN(out)} \dots (3.25)$$

Because both input signal power and input noise power are dissipated within the same resistance R_G ; and the output signal power and output noise power are dissipated within the same resistance R_L , the power ratios may be replaced by voltage-squared ratios. Although mean values of the noise components are zero, the mean square values exist, so that it becomes convenient to write the complete expression in terms of mean squares:

$$NF = \frac{\overline{v_S^2(in)}/\overline{v_N^2(in)}}{\overline{v_S^2(out)}/\overline{v_N^2(out)}} \dots (3.26)$$

where

$$\begin{aligned} \overline{v_S^2(in)} &= \text{mean square value of input signal voltage} \\ \overline{v_S^2(out)} &= \text{mean square value of output signal voltage} \\ \overline{v_N^2(in)} &= \text{mean square value of input noise voltage} \\ \overline{v_N^2(out)} &= \text{mean square value of output noise voltage} \end{aligned}$$

but

$$\frac{\overline{v_S^2(out)}}{\overline{v_S^2(in)}} = A_V^2, \text{ the voltage gain}$$

so that equation 3.26 becomes:

$$NF = \frac{\overline{v_N^2(out)}}{A_V^2 \overline{v_N^2(in)}} \dots (3.27)$$

In this expression two mean-square noise voltages appear, and these may be interpreted:

(a) $\overline{v_N^2(in)}$ is the Johnson noise which arises in the resistance R_G and is applied to the input terminal. This is given by the well-known Nyquist equation:

$$\overline{v_N^2(in)} = 4 k T R_G \Delta f \dots (3.28)$$

where

k = Boltzmann's Constant
 T = temperature in $^{\circ}K$
 Δf = bandwidth over which the noise is measured.

(b) The noise at the output is the sum of the amplified Johnson noise at the input plus the noise arising within the amplifier, v_N :

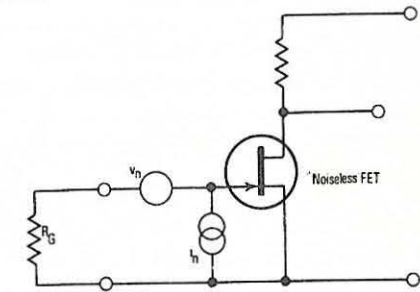
$$\overline{v_N^2(out)} = A_V^2 4k T R_G \Delta f + \overline{v_N^2} \dots (3.29)$$

Putting equations 3.28 and 3.29 into equation 3.27, the noise factor becomes:

$$NF = 1 + \frac{\overline{v_N^2}}{A_V^2 \overline{v_N^2(in)}} = 1 + \frac{\overline{v_N^2}}{4 A_V^2 k T R_G \Delta f} \dots (3.30)$$

The only unknown in this expression is v_N , the noise generated within the amplifier. Several phenomena contribute to v_N , making it a frequency dependent quantity as will be seen later.

Figure 29. Noise voltage and current generator representation.



One of the most common methods of describing v_N , is by the use of equivalent noise voltage and current generators. Figure 29 shows a hypothetical noiseless amplifier preceded by noise generators v_n and i_n . If a resistance R_G is present at the input to the amplifier then:

$$v_N = A_V (v_n + i_n R_G) \dots (3.31)$$

because normally $R_G \ll R_{in}$ for a FET amplifier.

These are all instantaneous quantities, and as mean-square values are being considered, equation 3.31 must be re-written:

$$\overline{v_N^2} = A_V^2 \overline{(v_n + i_n R_G)^2} = A_V^2 (\overline{v_n^2} + \overline{i_n^2 R_G^2} + 2 \overline{v_n i_n R_G})$$

or

$$\overline{v_N^2} = A_V^2 (\overline{v_n^2} + \overline{i_n^2 R_G^2} + 2 \overline{v_n i_n R_G}) \dots (3.32)$$

Now

$$\overline{v_n i_n} = \gamma \sqrt{v_n^2} \sqrt{i_n^2} \quad \dots (3.33)$$

where γ is the correlation coefficient which is a measure of the degree of correlation, or mutual dependence between the two noise functions. Equation 3.33 does in fact define γ in this context:

$$\gamma = \frac{\overline{v_n i_n}}{\sqrt{v_n^2} \sqrt{i_n^2}} \quad \dots (3.34)$$

This definition is a special case (relevant to functions whose mean values are separately zero) of a more statistical definition. It simply says that for complete correlation ($\gamma = 1$) the mean of the product $v_n i_n$ is identical to the product of the two r.m.s. values; whereas for no correlation ($\gamma = 0$) the mean of the product would be zero.

Putting equation 3.33 into equation 3.32 gives:

$$\overline{v_n^2} = A_n^2 \left[\overline{v_n^2} + \overline{i_n^2} R_G^2 + 2 \gamma (\overline{v_n^2} \overline{i_n^2})^{1/2} R_G \right] \quad \dots (3.35)$$

Returning to equation 3.30, the noise factor now becomes:

$$NF = 1 + \frac{\overline{v_n^2}}{4 k T R_G \Delta f} + \frac{\overline{i_n^2} R_G}{4 k T \Delta f} + \frac{2 \gamma (\overline{v_n^2} \overline{i_n^2})^{1/2}}{4 k T \Delta f} \quad \dots (3.36)$$

In this expression, the bandwidth over which each noise generator is measured could reasonably be incorporated into the measurement itself, giving $\overline{v_n^2}/\text{Hz}$ and $\overline{i_n^2}/\text{Hz}$. If a true r.m.s. instrument were used, the directly measured voltage and current could be divided by $\sqrt{\Delta f}$ to give units of voltage-per-root-Hertz and current-per-root-Hertz, or in practical terms, nV/ $\sqrt{\text{Hz}}$ and pA/ $\sqrt{\text{Hz}}$.

These are units in which the noise generator values are normally quoted, but because $\sqrt{v_n^2}/\sqrt{\text{Hz}}$ and $\sqrt{i_n^2}/\sqrt{\text{Hz}}$ are cumbersome symbols, $\overline{e_n}$ and $\overline{i_n}$ are normally substituted. The units are also given which negate this ambiguity. Using $\overline{e_n}$ and $\overline{i_n}$ in this context, the noise factor of equation 3.36 becomes:

$$NF = 1 + \frac{1}{4kT} \left[\frac{\overline{e_n^2}}{R_G} + \overline{i_n^2} R_G + 2 \gamma \overline{e_n} \overline{i_n} \right] \quad \dots (3.37)$$

In the case of FET's the correlation coefficient can be taken as zero at audio frequencies and lower, for $\overline{i_n}$ represents the reverse gate-current shot noise, and

$\overline{e_n}$ the channel resistance Johnson noise plus the 1/f noise. Hence equation 3.37 simplifies to:

$$NF \approx 1 + \frac{\overline{e_n^2} + \overline{i_n^2} R_G^2}{4 k T R_G} \quad \dots (3.38)$$

The relative magnitudes of $\overline{e_n}$ and $\overline{i_n}$ are such that if $R_G < 10$ megohm, then $\overline{i_n^2} R_G^2 \ll \overline{e_n^2}$, so that:

$$NF \approx 1 + \frac{\overline{e_n^2}}{4 k T R_G} \quad \dots (3.39)$$

The noise factor NF is usually expressed in decibels, so that, being a power ratio, the resultant noise figure is:

$$\text{Noise Figure (dB)} = 10 \log_{10} NF \quad \dots (3.40)$$

From a practical point-of-view, a stage with a noise figure quoted at 3dB (for example), would simply mean that the S/N ratio at the input was twice as great as that at the output.

The disadvantage of the noise figure (or noise factor) is that it relates only to an amplifier having a given value of R_G . Conversely, the $\overline{e_n}, \overline{i_n}$ characterization is independent of R_G , and relates solely to the FET itself. Figure 30 gives a graphical relationship between $\overline{e_n}$, noise figure and R_G . It has been calculated assuming that $\overline{i_n}$ is zero, and should not be treated as an exact representation of the relevant relationships.

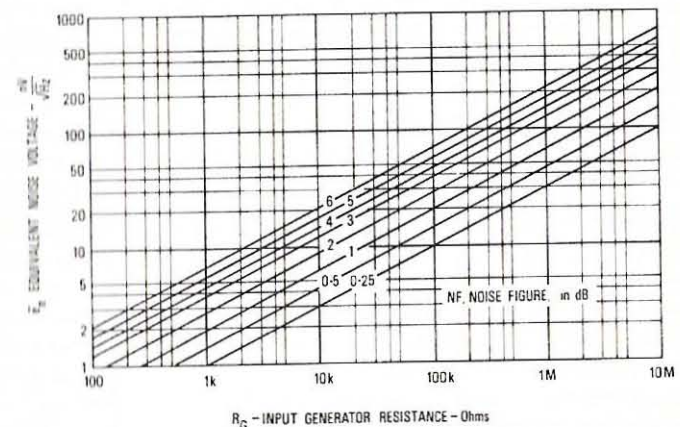


Figure 30. Noise Figure - noise voltage conversion chart.

If equation 3.38 is differentiated and equated to zero in order to determine the condition for minimum noise figure, it will be found that the resulting optimum value of R_G is:

$$R_G(NF \min) = \frac{\bar{e}_n}{\bar{i}_n} \quad \dots (3.41)$$

Notice that this does not imply minimal noise at the output, but only minimal noise figure — that is, minimum degradation of the signal in its passage through the amplifier.

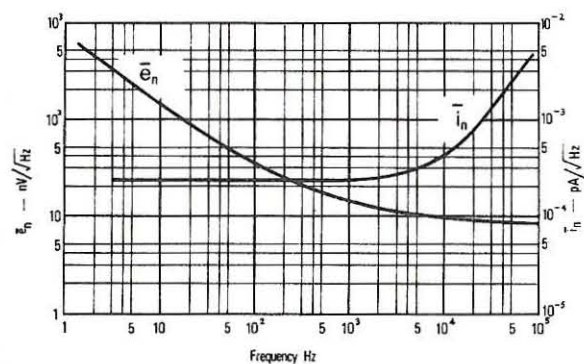


Figure 31. Variation of \bar{e}_n and \bar{i}_n with frequency for a typical FET.

Figure 31 shows how \bar{e}_n and \bar{i}_n vary for a typical FET. The rise in \bar{e}_n as the frequency is reduced is due to flicker, or $1/f$ noise. This is a little understood surface effect common to both FET's and bipolar transistors. FET's, however, usually exhibit lower flicker noise than do bipolars, and the relevant characteristic begins to be important at about 100 Hz for the former compared with 1 kHz for the latter.⁹

Equation 3.41 implies that if R_G is much lower than \bar{e}_n/\bar{i}_n , then the noise figure is liable to be high. For FET's, $R_G(NF \min)$ is invariably very large, so that if R_G is much less than 1 megohm, the possibility of using a bipolar transistor should be investigated. When a modern low-level planar bipolar transistor is run at a collector current of only a few micro-amps, it exhibits an input resistance of several megohms. It also has noise generator values which result in \bar{e}_n/\bar{i}_n ratios making for a minimal noise figure when R_G is several thousand ohms. There is consequently no point in using a FET input stage under these circumstances; the FET comes into its own when very high values of R_G are mandatory. (Usually R_G is a fixed design parameter, and it must be remembered that to increase its

value artificially to obtain a low NF is futile, because the noise generated by R_G itself is amplified and appears at the output. Hence the absolute value of noise will inevitably be greater if R_G is increased.)

Unlike the bipolar transistor, the noise generator within a FET is not a marked function of operating conditions. The only useful criterion is that a high g_{fs} (implying operation near I_{DSS}) makes for a low value of \bar{e}_n .

The application of feedback reduces internally generated noise by the same amount that the gain is reduced. In other words, **feedback cannot improve the signal-to-noise ratio**. It may, in fact, become worse, as the bandwidth improvement may allow a wider noise spectrum to appear, and the feedback resistors themselves will contribute to the total noise.

The designer is therefore virtually limited to choosing the correct device for his particular low-noise application, and here the manufacturer can be of considerable assistance. For example, the manufacturer can specify the correct device for given circuit conditions, and can take into account the maximum allowable value of \bar{e}_n , especially in cases where the correct device is not immediately apparent from printed data information. Further, in particularly exacting cases, the manufacturer can supply trial samples with recorded noise data, enabling the designer to empirically determine the highest value of \bar{e}_n acceptable in his circuit.

3.13 MOSFET's in amplifier stages

MOSFET's tend to exhibit much higher noise figures than junction FET's, and so are rarely used (in discrete form) as linear amplifiers. There are a few exceptions to this rule, such as their usage in high-grade electrometer amplifiers, where extremely high input resistances are required.

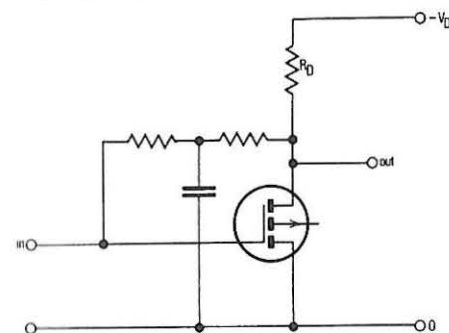


Figure 32. (a) Self-biased enhancement MOSFET stage.

Another application is where circuit simplicity and economy of components is important to the design. Figure 32 (a) shows that when the gate and drain of an

enhancement MOSFET are biased in the same polarity, it is necessary only to take the gate to the drain to achieve bias stability. (The a.c. signal must, of course, be decoupled). The relevant output characteristics are shown in Figure 32 (b), along with the locus of the working point — simply given by $V_{GSQ} = V_Q$. Figure 32 (c) shows the simplicity of a cascade of enhancement MOSFET's, and indicates how a feedback loop may be used for bias stabilization purposes.

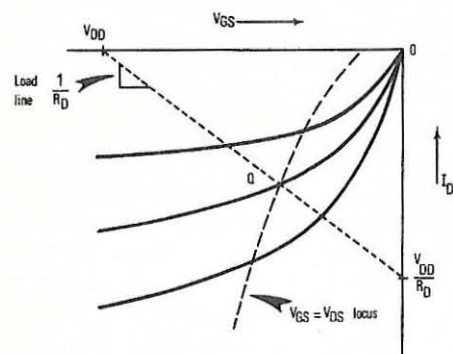


Figure 32. (b) Output characteristics and working point for self-biased enhancement MOSFET.

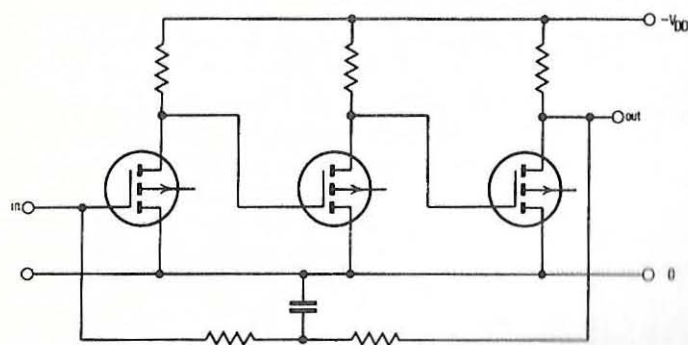


Figure 32. (c) Three-stage MOSFET amplifier with overall feedback biasing

Where an incoming signal fluctuates around ground potential, it may be convenient to use a depletion MOSFET as the input device. As was shown in Figures 17 (b) and (d), the quiescent drain current will be held at $I_Q = I_{DSS}$ under these circumstances.

Summary

The foregoing forms the basis upon which to design simple FET amplifier stages from both the biasing and amplification aspects. Usually bipolar transistor stages follow a FET input stage because they are capable of higher voltage gains. The FET, however, is invaluable in that it provides a high input impedance and contributes very little noise if correctly selected, and if the circuit is properly designed.

VOLTAGE-CONTROLLED RESISTORS, CURRENT-LIMITERS AND D.C. AMPLIFIERS

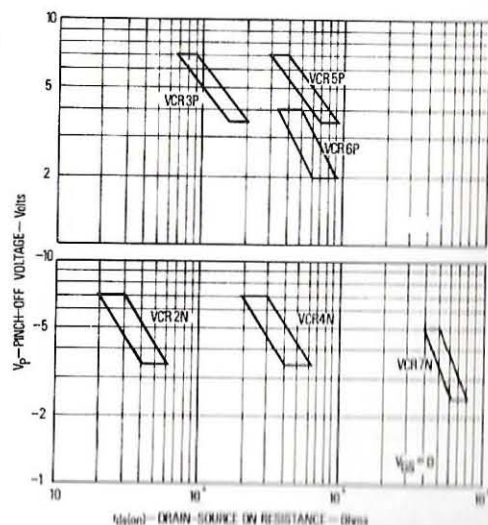
4.1 The voltage-controlled resistor (VCR)

Under the correct operating conditions the channel of a FET behaves as an almost pure ohmic resistor whose value is a function of the gate voltage V_{GS} . This unique property can be deduced from Figure 12(a), page 22, where the output characteristics, very near the origin, of a Siliconix 2N2609 P-channel FET are reproduced. Here, the curves all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance r_{ds} is essentially the same as the d.c. or chord resistance r_{DS} , and this is a function only of V_{GS} .

Figure 12 (a) also shows that for very small excursions of V_{DS} , the device can be considered fully bi-lateral; that is, the drain voltage can swing positive or negative with respect to the source¹⁰. This is because the junction can be very slightly forward-biased before any significant gate current flows.

Assuming that the FET is operated very near the origin, then using small-signal measuring techniques, plots of channel resistance versus gate voltage can be made¹¹, as illustrated in Figure 12 (b). The lowest resistance presented by a

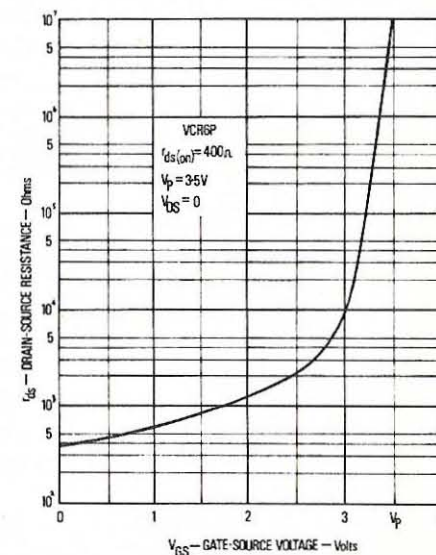
Figure 33. V_p and $r_{ds(on)}$ spreads for a range of P-channel (top) and N-channel (bottom) VCR's.



channel, $r_{ds(on)}$, (which may also be written $r_{DS(on)}$ or R_O), occurs when $V_{GS} = 0$; its value is therefore dictated by the geometry of the device. For example, a wide channel will exhibit a low $r_{DS(on)}$ and also a high I_{DSS} , which may be interpreted to mean that a high I_{DSS} device should be chosen for those applications where a low $r_{DS(on)}$ is required. Approximately, $r_{DS(on)}$ is given by $\frac{1}{g_{fso}}$, so that the data sheet value of g_{fso} may be used to make a crude determination of this parameter even though it may not be given explicitly.

A range of FET's designed specifically for use as voltage-controlled-resistors is the Siliconix VCR group. This includes both P and N-channel units having values of $r_{DS(on)}$ from 60 ohms (max) to 4000 ohms (min), the relevant spreads being given in Figure 33. A typical curve showing the variation in r_{ds} as a function of V_{GS} for one of this series appears in Figure 34 below.

Figure 34. Variation in r_{ds} as a function of V_{GS} for a Siliconix VCR6P P-channel VCR device.



From Figure 12 (b), page 23, and Figure 34 above, it will be seen that over a range of about one decade above $r_{DS(on)}$, the rise in r_{ds} is very nearly exponential (the characteristic being almost a straight line and the y-axis being logarithmic). Above this, however, the rise in r_{ds} becomes very rapid, and for most VCR purposes, unusable. The law relevant to the exponential region is, approximately,

$$r_{DS} = r_{DS(on)} e^{\lambda V_{GS}} \quad \dots (4.1)$$

where λ is a constant which depends largely on the pinch-off voltage of the

relevant device. (An empirical rule of thumb is that typical FET's follow the approximation:

$$g_{os} \approx g'_{os} \left(1 - \frac{V_{gs}}{V_p}\right)$$

where g'_{os} is defined at $V_{gs} = 0$. This approximation is valid up to about $V_{gs} = 0.6V_p$.)

Within the range $r_{DS(on)} < r_{DS} < 10r_{DS(on)}$ it is reasonable to match devices, producing dual VCRs, or even quads; but above this region matching becomes nearly impossible.

The channel resistance of the VCR is, like that of all FET's, temperature dependent, and this is due to two effects: the decrease in carrier mobility with temperature tends to increase r_{DS} , and the fall in the gate-channel contact potential tends to decrease it. Consequently, the channel resistance (like the channel current) passes through a zero temperature coefficient point at some value of V_{GS} , as is clearly demonstrated in Figure 35. The temperature coefficient of $r_{DS(on)}$ is about 0.7% per °C. for P-channel devices (of which the VCR6P of Figure 35 is an example) and about 0.5% per °C. for high- V_p N-channel

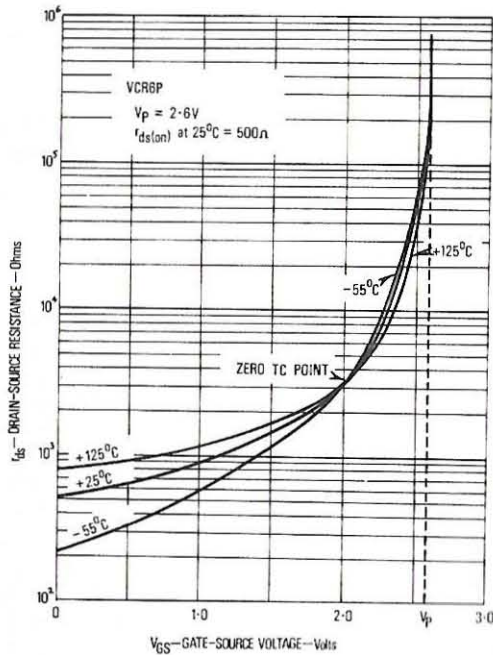


Figure 35. Temperature dependence of r_{DS} .

units. The FET geometry most suitable for VCR applications is that involving a long gate, since these types usually follow theoretical predictions more closely. The VCR6P and VCR10N - 13N, are long gate FET's. If uniformity of device characteristics is required these types should be specified. It is this uniformity that enables the manufacturer to offer matched pairs and quads, of which the VCR11N - 13N are examples.

It should be borne in mind that a long gate structure also leads to increased inter-electrode capacitances, thereby reducing the bandwidth of the device.

4.2 Applications of the VCR

The simplest way a VCR may be used is shown in Figure 36 (a), where a voltage divider attenuator is shown wherein the output voltage is:

$$v_{out} = \frac{v_{in} r_{DS}}{R + r_{DS}} \quad \dots (4.2)$$

It is assumed here that v_{out} is not so large as to take the VCR out of the linear resistance region. It is also assumed that there is no load shunting r_{DS} .

The lowest value which v_{out} can assume is obviously:

$$v_{out(min)} = \frac{v_{in} r_{DS(on)}}{R + r_{DS(on)}} \quad \dots (4.3)$$

while the highest is:

$$v_{out(max)} = v_{in}$$

for r_{DS} can be extremely large.

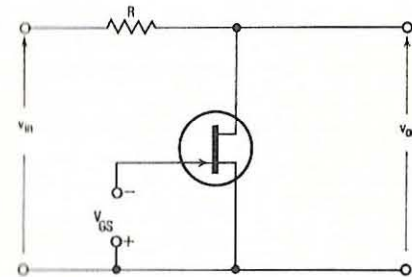


Figure 36a Simple VCR attenuator

Figure 36 also includes some other simple configurations. Diagram (b) shows two

cascaded attenuator stages, while diagrams (c) and (d) indicate how phase advance and retard circuits may be implemented. Figure 36 (e) shows a P-channel VCR used as a variable load for a photo-multiplier. This application has been chosen

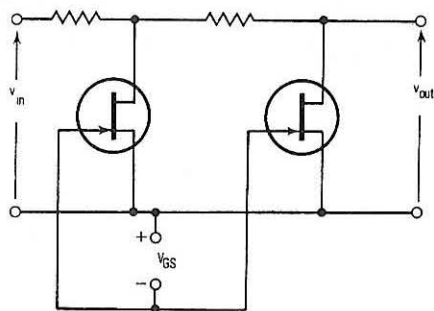


Figure 36b. Cascaded VCR attenuator

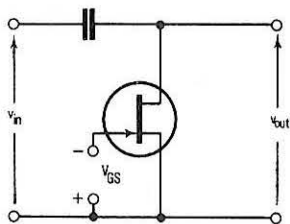


Figure 36c VCR phase advance circuit

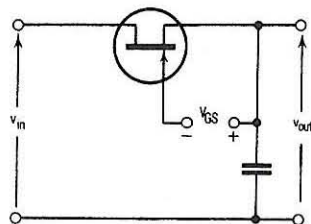


Figure 36d VCR phase retard circuit

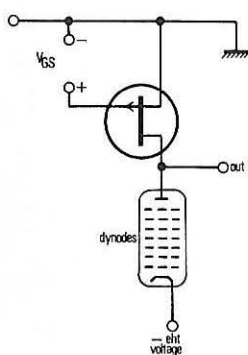


Figure 36e VCR photomultiplier load

because the low anode current of a photo-multiplier (usually 1 microamp or less if fatigue effects are to be avoided) implies that the VCR will always work in the linear region near the origin. Clearly, it may be also used as an 'active' load for any other device, including bipolar or field effect transistors, but if the relevant currents and voltage drops are high level, the VCR operating point may move out of the linear region, and distortion will result. Figure 36 (f) is a useful gain control circuit, provided that this latter limitation is kept in mind when such a stage is designed.

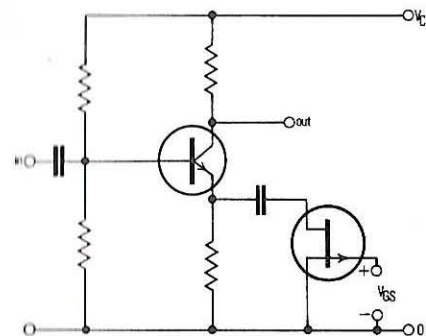
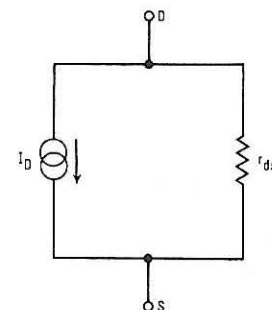


Figure 36f VCR gain control

4.3 The current-limiter (CL)

A FET used as a current generator¹² must be operated well into the saturation or pinch-off region (which is the converse of the case for the VCR). Figures 4 and 5, pages 9-10, showed that in this region the incremental channel resistance presented is very high, and that the direct current flowing is dependent predominantly upon V_{GS} . Therefore, at low frequencies where the interelectrode

Figure 37 Equivalent circuit of FET used as a current source.



capacitances are unimportant, the equivalent circuit is as shown in Figure 37, where I_D is given by the usual square-law equation:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

The incremental channel resistance r_{ds} is large, so that the device approximates to a V_{GS} – dependent current generator.

If the gate is connected to the common line, as shown in Figure 38, the device becomes an independent current generator, and because

$$V_{GS} = I_D R_S,$$

then,

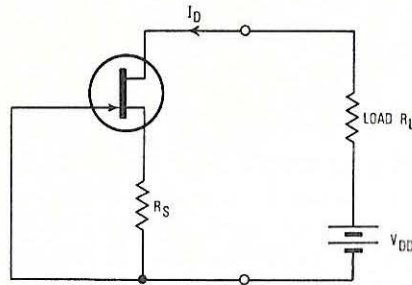
$$I_D = I_{DSS} \left[1 - \frac{I_D R_S}{V_P} \right]^2$$

giving

$$R_S = \frac{V_P}{I_D} \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right] \quad \dots (4.4)$$

When $R_S = 0$, then $I_D = I_{DSS}$, which is the largest current which can pass.

Figure 38 *Constant-current connection*



A two-terminal current-limiter consists of a FET having an internal resistor R_S , which may be fabricated on the same chip. Conversely, R_S may be omitted altogether, when the gate is connected directly to the source. A series of such devices is the Siliconix CL2210 to CL4720 range, and Figure 39 shows how temperature affects the nominal current for each device in this range. The temperature coefficient varies from a positive to a negative value depending on the nominal current, and for some devices is very small indeed. This is another manifestation of the fact that temperature variations in channel conductivity and junction potential work in opposition insofar as I_D is concerned, with the result that near-cancellation is achieved by certain devices working under the correct conditions.

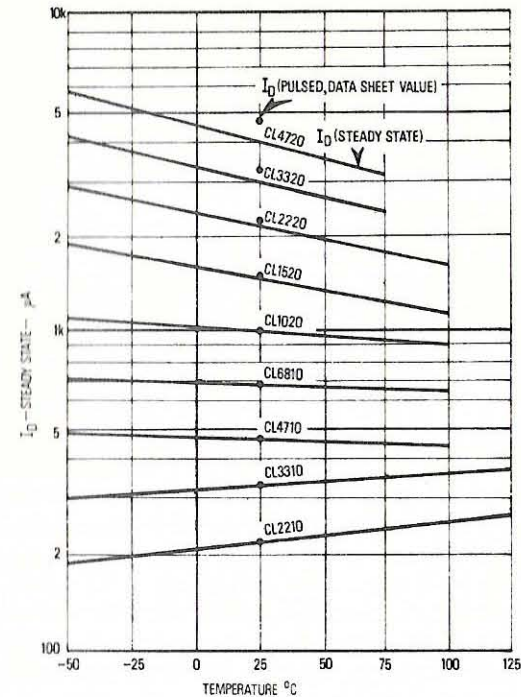


Figure 39 *Temperature variation of I_D for a range of current limiters.*

It is self-evident that the drain-source voltage of the device must exceed pinch-off voltage in order that it should work in the saturation region, i.e. $|V_{DS}| > |V_P|$. In the case of the CL, the relevant pinch-off voltage is called the limiting voltage, V_L , and this is a function of the geometry of the device. Normally, V_L is given in the data sheets, and the circuit designer must always establish that the CL is never required to work at a voltage lower than this value.

4.4 Applications of the current limiter

The most obvious applications of a constant-current device are in timing and linearizing circuits. Figure 40 shows a typical Unijunction transistor timing circuit, where the capacitor C is charged linearly via a CL. The output pulses will be spaced by a time t , where

$$t = \frac{CV}{I_{CL}}$$

where V is the voltage at which the Unijunction transistor fires.

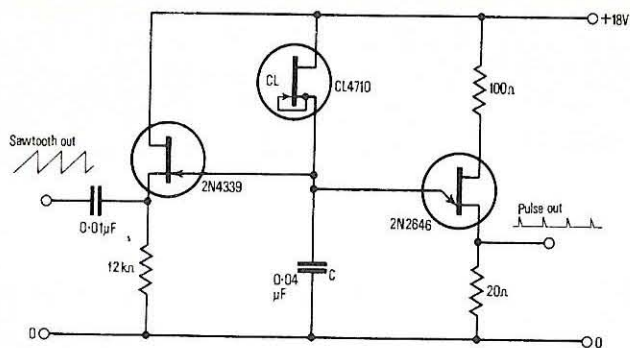
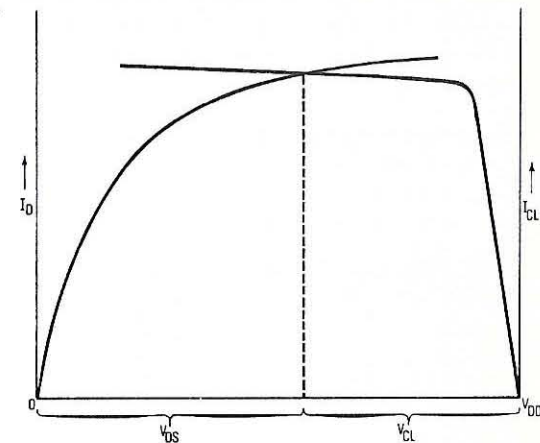


Figure 40 Sawtooth wave generator using a CL. For $C = 0.04 \mu F$, and using a Siliconix CL4710, p.r.f. is about 1 kHz.

Because the capacitor charges linearly, a saw-tooth waveform appears across it, and this waveform may be extracted by using a (very high input resistance) FET buffer stage as shown. If it is desired that the repetition frequency of the circuit should be variable, then either the value of C , or the constant current I_{CL} , must be adjustable. Normally, it is convenient only to switch in fixed capacitances, but I_{CL} can be made continuously variable by using not a two-terminal CL, but by connecting a FET as in Figure 38 with R_S a variable resistor.

The two-terminal CL is more appropriate where the existence of a large, but finite, internal resistance r_{ds} is advantageous. Figure 41 (a) shows how a CL may be connected as a drain load, but Figure 41 (b) demonstrates that such a connection is not very stable insofar as biasing is concerned. This is because the channel characteristics of the amplifier device and the CL cross at a small angle, so that temperature variations can easily move the working point out of the saturation region of either the amplifier device or the CL. However, if temperature

Figure 41b The working point for Figure 41a.



variations are liable to be small, the voltage gain of such a combination is very high, because, for a FET

$$A_V \approx -g_{fs} \cdot R_L = -g_{fs} \cdot r_{ds}(CL)$$

The use of a CL as the load of an emitter (or a source-follower) is much more reasonable from a biasing point-of-view, (Figure 42), and a logical extension of this application is the replacement of the common resistor of a difference amplifier, or a long-tailed pair, as shown in Figure 46, page 71. Here, because r_{ds} for the CL is very large, the common-mode rejection properties of the pair are rendered very good indeed. This is the fundamental configuration used in d.c. amplifiers, which form the subject matter of the next section.

Figure 41a The CL as an 'active' drain load.

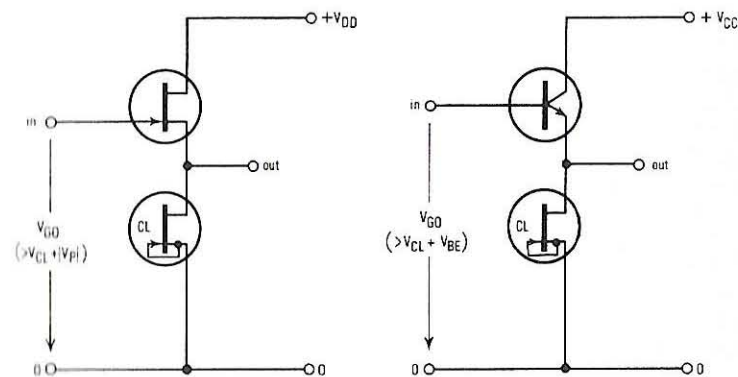
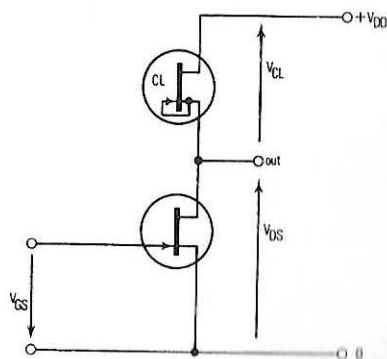
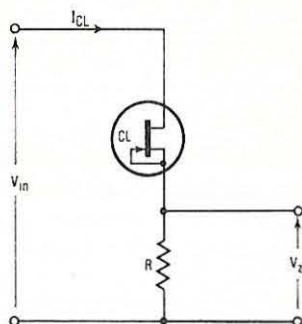


Figure 42 The CL as an 'active' source or emitter load.

In point of fact, difference amplifiers are often used as voltage comparators (in stabilized power supply circuits for example) where one input is derived from a Zener diode. In cases where a voltage smaller than three volts is desired; or where a low noise voltage source is mandatory, the Zener diode may be conveniently replaced by a CL/resistor combination as shown in Figure 43. Here, the reference voltage appears across the resistor and has a value $I_{CL}R$. The noise generators involved are the thermal noise of the resistor in parallel with the thermal noise of the current-limiter channel. This combination is usually some orders of magnitude lower than the noise associated with a Zener diode.

Figure 43 CL/resistor combination replacing Zener diode.



4.5 The D.C. Amplifier

The fundamental problem involved in the amplification of very slowly fluctuating (or "d.c.") signals is that the inherent drift of the amplifier with changes in temperature, or with the passage of time, can often be of the same order of magnitude as the input signal itself. In the case of a bipolar transistor, for example, changes in I_{CBO} , V_{BE} and h_{FE} with temperature all conspire to alter the collector current in the same sense. The channel current in a FET, however, is affected in opposite senses by the change in channel conductivity and the change in junction potential with temperature. Working under ideal conditions, therefore, a FET can exhibit a channel current temperature coefficient of almost zero. Unfortunately, these conditions are somewhat different for each unit, though approximations are given by equations 3.19 page 47.

(i.e. $|V_{GSQ}(Z)| \approx |V_P| - K$; being 0.63 or 0.9 for P and N-channel respectively)

A better solution is that offered by the matched pair approach¹³, where the drifts of two almost identical FET's are arranged to cancel each other as far as possible. Unlike bipolar transistors, two FET's fabricated next to each other on one silicon slice are unlikely to be closely similar, so that it is necessary to test each structure individually and choose pairs which match within pre-determined limits. Siliconix matched pairs are selected by means of a unique computerized version of this procedure, and are then mounted in close proximity upon single,

multi-lead headers so that temperature differentials are minimized. The latter precaution is important, because all parameters vary with temperature, and those of each half of a matched pair must not only be closely similar at one temperature, but must closely track each other as temperature varies. This means, of course, that the temperatures of the two structures must also be similar under operating conditions.

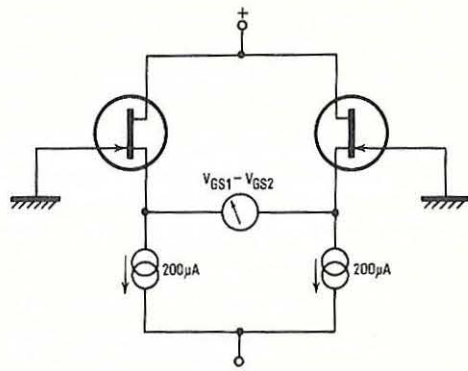
Some actual parameters for the Siliconix 2N5515 or 2N5520 dual N-channel FET will illustrate the degree of matching which may be achieved:

Parameter	Test conditions	Min	Max
I_{DSS1}	$V_{DS} = 20V$		
I_{DSS2}	$V_{GS} = 0$	0.95	1
$V_{GS1} - V_{GS2}$	$V_{DG} = 20V$ $I_D = 200\mu A$	—	5 mV
$\frac{\Delta(V_{GS1} - V_{GS2})}{\Delta T}$	$V_{DG} = 20V$ $I_D = 200\mu A$ $T_A = +25^\circ C \quad T_B = +125^\circ C$ or $T_A = -55^\circ C \quad T_B = +25^\circ C$	—	$5\mu V/^\circ C$
g_{fs1}	$V_{DG} = 20V$		
g_{fs2}	$I_D = 200\mu A$ $f = 1kHz$	0.97	1

In this table, the first entry guarantees that when $V_{DS} = 20V$, then the two values of I_{DSS} will be within 5% of each other. All the other parameters are the results of tests carried out at constant values of I_D which are derived from highly stable constant-current generators. Figure 44 shows how the difference in gate-source voltage is measured under conditions of constant I_D : the two gates are grounded, and the difference between the source voltages is measured as the two current generators force $200\mu A$ through each channel. This measurement is clearly $(V_{GS1} - V_{GS2})$, which for the 2N5515/20 is guaranteed to be below 5mV. If now the FET is heated and cooled in an environmental chamber, the average drift in $(V_{GS1} - V_{GS2})$ with temperature can be determined. The third entry in the table quotes $5\mu V/^\circ C$ for this measurement, and shows the actual temperatures over which the average rate of change is valid. Temperature drift, like noise, is usually dominated by the input stage of an amplifier, which

makes this measurement one of the most useful parameters of a dual FET.

Figure 44 Method of measuring gate-source voltage.



The ratio of the two values of g_{fs} is guaranteed as shown in the fourth entry. For the 2N5515/20, the two halves have g_{fs} values within 3% of each other, which makes for considerable design simplification.

The application of matched pairs to difference amplifiers will be considered in the next section; meanwhile, a second approach to d.c. amplification must be mentioned. This is the chopper approach, wherein the d.c. signal is chopped into segments (modulated), amplified by an inherently drift free a.c. amplifier, then reconstituted (demodulated) into its original form. Figure 45 shows how this is accomplished, and the chopper itself may consist of (a) an electro-mechanical relay-type unit (b) bipolar transistors (c) field effect transistors or (d) one FET and one bipolar. The advantages and disadvantages of these choppers will be briefly discussed, and the FET chopper treated in detail in chapter 6.

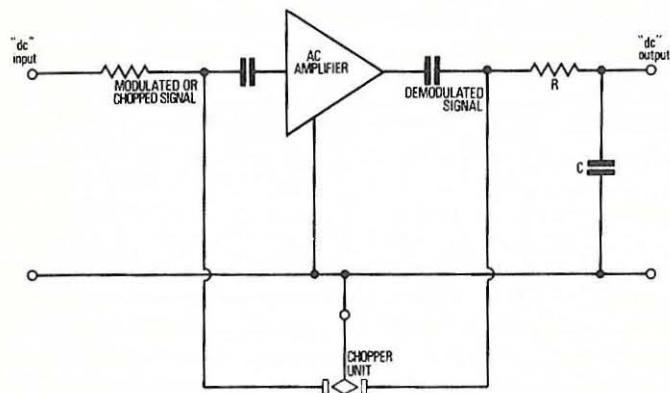


Figure 45 The chopper approach to 'd.c.' amplification.

4.6 The Difference Amplifier

This configuration, sometimes called a long-tailed pair, is shown in Figure 46. If the common resistance R_x is large, then it essentially defines the total current ($I_{D1} + I_{D2}$), and establishes that if I_{D1} changes by an amount ΔI_D , then I_{D2} also changes by this amount, but in the opposite sense. That is, $(I_{D1} + I_{D2}) = I_x$, which is constant.

For the above statement to be even approximately true, R_x would have to be very large indeed, as would $-V_{DD}$.

Both of these requirements are inconvenient, but the substitution of R_x by a CL as shown in Figure 46 does much to solve the problem as it is an approximate current generator which passes an adequate quiescent current, but presents a very high incremental resistance $r_{ds}(CL)$.

If the CL is considered to be a perfect current generator, then the difference gain of the circuit can be determined without difficulty by observing that $(I_{D1} + I_{D2}) = I_{CL}$, which is constant. If this is the case, then for small changes in I_{D1} and I_{D2} ,

$$(I_{D1} + \delta I_{D1}) + (I_{D2} + \delta I_{D2}) = I_{CL}$$

so that

$$\delta I_{D1} = -\delta I_{D2}$$

which in turn means that

$$\delta V_{GS1} = -\delta V_{GS2}$$

(the gates will be biased either through shunt resistors or through the drive generator itself.)

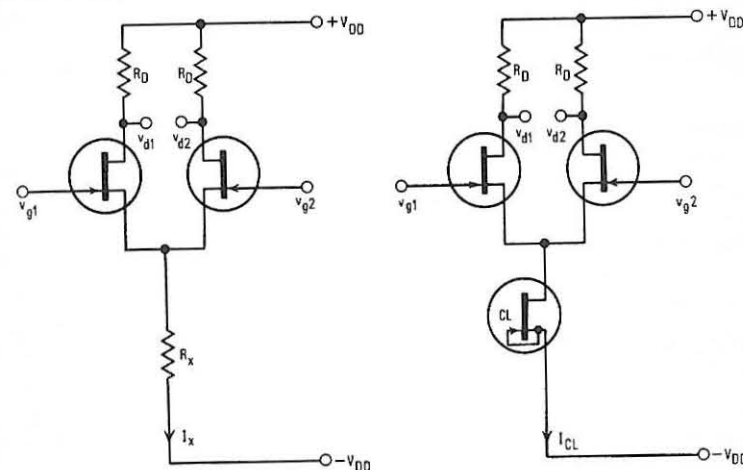


Figure 46 Replacement of the common resistor of a difference amplifier by a CL.

In other words, if the inputs at each gate are v_{g1} and v_{g2} , then $(v_{g1} - v_{g2}) = 2v_{gs} = v_{gg}$. Hence, the output voltage between the drains is:

$$v_{dd} = (v_{d1} - v_{d2}) \simeq R_D(i_{d1} - i_{d2}) = R_D g_{fs}(v_{gs1} - v_{gs2}) \\ = R_D g_{fs} v_{gg}$$

giving

$$A_{v(dd)} = \frac{v_{dd}}{v_{gg}} = R_D \cdot g_{fs} \quad \dots (4.5)$$

which is the same expression as for a simple CS stage.

The common-mode gain may be equally easily obtained by observing that for similar signals at each gate, the drain currents will change in the same sense, so that if the CL is imperfect (that is, $r_{ds(CL)}$ is not infinitely great,) there will be a nett change in the current passing through the CL. Because the signals at each are the same, and the two FET's are assumed to be perfectly matched, the two halves of the circuit may be treated as separate degenerate CS stages each with a source resistor of value $2r_{ds(CL)}$. The gain of each, and hence the common-mode gain is therefore simply that of equation 3.16:

$$A_{v(CM)} = \frac{v_{d1}}{v_{g1}} = \frac{v_{d2}}{v_{g2}} = \frac{-g_{fs} R_D}{1 + g_{fs} \cdot 2r_{ds(CL)}}$$

and because $2r_{ds(CL)}$ is very large, this approximates to:

$$A_{v(CM)} \simeq -\frac{R_D}{2r_{ds(CL)}} \quad \dots (4.6)$$

This is clearly a very low common-mode gain — much lower in fact than would be the case for any realistic value of R_X if the circuit of Figure 46 (a) were used. A low common-mode gain is extremely desirable from the point of view of temperature drift, because changes in I_D , V_{GS} and g_{fs} can be treated as common-mode signals if they are all the same for both FET's. This is the reason why the two FET's must be closely matched for both initial values and for temperature tracking. Also, the simple expressions obtained above depend entirely upon perfect identity between the FET's. Had differences been taken into account, most unweildy expressions would have resulted.

The common-mode rejection ratio, or discrimination factor, may be defined as the ratio of difference gain to common-mode gain, and is therefore given approximately by:

$$CMR = \frac{A_{v(dd)}}{A_{v(cc)}} \simeq 2g_{fs}r_{ds(CL)} \quad \dots (4.7)$$

This equation has been derived for perfectly matched FET's. A more comprehensive derivation, taking into account mismatching would indicate that CMR is a more complex function of the relative values of g_{fs} and g_{os} . For example, the 2N5515 series has a long gate geometry resulting in an inherently low g_{os} . This provides a better g_{os} match, allowing the manufacturer to guarantee a minimum CMR of 100 dB. (This assumes ideal circuit conditions).

HIGH FREQUENCY AMPLIFIERS AND MIXERS

5.1 Introduction

The FET has several advantages as a high frequency device if compared to the bipolar transistor. Firstly, it exhibits less noise up to and including the UHF range. Secondly, because the input resistance is very large (for the CS stage), it dissipates negligible power and also enhances the performance of any tuned input circuit. Thirdly, because it has a square-law transconductance curve, it is not only capable of handling much greater input voltage swings than the bipolar, but will do so with much less generation of unwanted components at the output. The following sections briefly describe the problems encountered in h.f. circuit design using FET's, and will include some practical circuits.

5.2 The problem of h.f. amplification

In Sections 3.5 and 3.6 it was shown that when signal frequencies rise to only the audio region, the inter-electrode capacitances of the FET begin to present reactances low enough to adversely affect the performance of the device — particularly with respect to input impedance.¹⁴ For the CS stage, the Miller Effect provides the dominant capacitance, so that the input impedance is largely a reactance of value

$$X_{in} = \frac{1}{2\pi f C_{in}}$$

where $C_{in} = C_{iss} - A_v C_{rss}$... (3.8b)
from page 40

For the CS connection this will be as low as a few thousand — or even a few hundred ohms at frequencies in the megahertz region. For the source-follower, and more particularly for the common-gate connection, the Miller capacitance is much reduced. For this reason the CG configuration is in common use in h.f. amplifiers. The reverse capacitance of a FET, apart from lowering the input reactance, feeds back signals from the output to the input, possibly contributing to instability — especially if the load itself is reactive. Consequently much of the design effort in h.f. amplification is directed towards the reduction of the effects of this reverse capacitance, such efforts being made by both the manufacturer and the designer: the former by fabricating geometries with low inter-electrode capacitances, and the latter by choosing optimum circuit configurations. Some of these techniques are:—

1. Employment of standard h.f. circuit techniques — i.e. the inclusion of inter-electrode capacitances as part of the resonant circuits and the provision of adequate screening between input and output sides.
2. Use of the common-gate configuration where possible. Here, apart from the absence of phase reversal, the capacitance between input and output is C_{ds} , which is extremely small — so leading to a much lower Miller capacitance than for a CS stage. A similar result can be obtained by combining two FET's in the cascode connection.
3. Neutralization of the FET, which involves shunting the Miller capacitance with an inductive circuit, so producing a rejector circuit at the resonant frequency. This (as explained later) results ideally in the unilateralization of the amplifier — i.e. the removal of most of the internal feedback near the rejection frequency.

These circuit techniques, along with the correct choice of FET, make possible the design of h.f. amplifiers which compare very favourably with similar circuits using bipolar transistors and which can be highly stable under all working conditions. Sections 5.3 et seq describe some of the techniques, and include discussion of the Linvill-Gibbons criteria for h.f. stability. The question of biasing is not discussed, as it is usual in h.f. amplifiers to employ chokes and transformers, where the 'dead' ends of the relevant winding are simply taken to properly decoupled biasing points. The low resistance of these windings ensures that direct voltage drops are negligible, so that biasing methods already discussed are entirely valid under these circumstances.

5.3 The high-frequency FET

Short-circuit admittance (or y-parameters) are particularly useful in h.f. calculations, and they refer to the 2-port equivalent circuit of Fig. 47. The equations describing this equivalent circuit are, referring to the CS configuration:

$$I_{in} = Y_{is} E_{in} + Y_{rs} E_{out}$$

... (5.1 a)

$$I_{out} = Y_{fs} E_{in} + Y_{os} E_{out}$$

... (5.1 b)

where E_{in} and I_{in} are the input signal voltage and current,
and E_{out} and I_{out} are the output signal voltage and current.

If the output is short-circuited to a.c. (that is, if a capacitor shunts the output signal), then measurements at the input will give:

$$Y_{is} = \frac{I_{in}}{E_{in}(E_{out} = 0)}$$

= input admittance with output s/c

and

$$Y_{fs} = \frac{I_{out}}{E_{in}(E_{out} = 0)}$$

= forward transconductance with output s/c

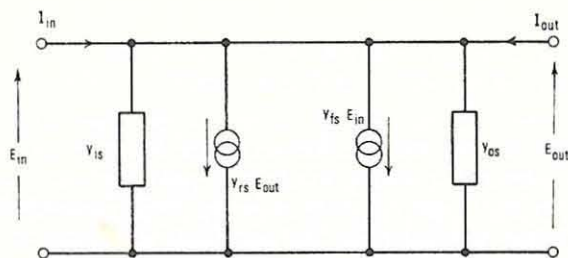


Figure 47 The CS y-parameter equivalent circuit.

If the input is similarly short-circuited to a.c., and a signal applied at the output the remaining y-parameters may be measured:

$$y_{rs} = \frac{I_{in}}{E_{out}(E_{in} = 0)} = \text{reverse transadmittance with input s/c}$$

and

$$y_{os} = \frac{I_{out}}{E_{out}(E_{in} = 0)} = \text{output admittance with input s/c}$$

Each of these parameters is a complex quantity, and may be derived from a 'physical' equivalent circuit which is rather more comprehensive than that previously given in Figure 16, page 27. Such an equivalent circuit, and expressions for the y-parameters in terms of its components, will be found in Reference 14.

The y-parameters are, of course, functions of frequency, and are so described in the data sheets. Numerical values are given for specified working conditions, and graphs are often included from which values at other frequencies may be determined. Typical of such graphs are those of Figure 48, which relate to the 2N5397. Notice that each y-parameter is specified in terms of its real and imaginary component. This approach is useful in that it enables stability calculations to be made as will be shown later.

In Figure 48 it will be seen that the frequency scale rises to 1000 MHz. For all practical applications much above 600 MHz, however, lead and header capacitances make the encapsulated device unusable, and it becomes necessary to employ the flip-chip version (FC102) along with strip line techniques. Such methods will carry the useful performance of the FET up to about 1.5 GHz.

For the common-gate configuration, y-parameters also exist, and though the equivalent circuit will remain unchanged, the numerical values of the parameters will be different. These parameters, y_{ig} , y_{rg} , y_{fg} and y_{og} , may also be expressed in terms of equivalent circuit parameters,¹⁴.

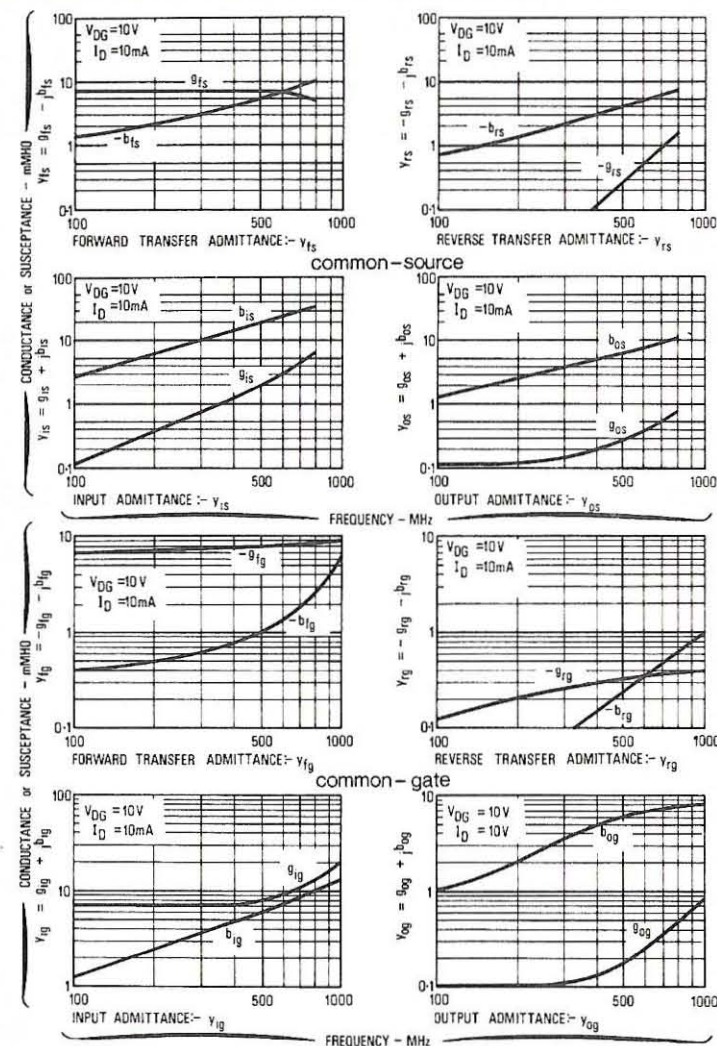


Figure 48 y-parameters for the Siliconix 2N5397.

Graphs giving CG y-parameter values for the 2N5397 also appear in Figure 48. At the lower frequencies, it is reasonable to measure C_{iss} and C_{rss} : for the 2N5397 working at 1 MHz these are 5 pF(max) and 1.2 pF(max) respectively when $V_{DG} = 10V$ and $I_D = 10mA$

The noise figure is also quoted, and often graphed, in the data sheets; it is largely a function of I_n , this being the dominant generator at high frequencies. For the 2N5397 the noise figure is 3.5 dB(max) at 450 MHz.

5.4 Neutralization

It has been explained that in order to negate the effect of C_{gd} in the CS h.f. amplifier, it is necessary only to shunt the gate/drain leads with an inductive circuit. Because the CS FET and its neutralizing path are in parallel, it is possible to define a set of y-parameters which relate to the FET taken along with this neutralizing path. This is done simply by adding the matrix of the FET to the matrix of the neutralizing path. That is:

$$\begin{bmatrix} Y_{is} & Y_{rs} \\ Y_{fs} & Y_{os} \end{bmatrix} + \begin{bmatrix} Y_N & -Y_N \\ -Y_N & Y_N \end{bmatrix} = \begin{bmatrix} Y_{is} + Y_N & Y_{rs} - Y_N \\ Y_{fs} - Y_N & Y_{os} + Y_N \end{bmatrix}$$

Hence the equations to the composite 2-port network become:

$$I_{in} = (Y_{is} + Y_N) E_{in} + (Y_{rs} - Y_N) E_{out}$$

$$I_{out} = (Y_{fs} - Y_N) E_{in} + (Y_{os} + Y_N) E_{out}$$

or

$$I_{in} = Y'_{is} E_{in} + Y'_{rs} E_{out} \quad \dots (5.2a)$$

$$I_{out} = Y'_{fs} E_{in} + Y'_{os} E_{out} \quad \dots (5.2b)$$

where the primed y-parameters refer to the composite network.

Clearly if perfect neutralization takes place so that the circuit becomes unilateral, then $Y'_{rs} = 0$. That is:

$$Y_N = Y_{rs}$$

and no feedback occurs.

In practice, Y_{rs} is largely capacitive, so making the neutralizing path largely inductive. Both paths must have the same reactance at the frequency for which the amplifier is to be designed. That is:

$$2\pi fL = \frac{1}{2\pi f C_{gd}} \quad \text{or} \quad L = \frac{1}{4\pi^2 f^2 C_{gd}} \quad \dots (5.3)$$

This is normally achieved by using a variable inductor and connecting it in series with a large capacitor for d.c. isolation purposes. Such a circuit is given in Figure 49 and is described in Section 5.5 below.

5.5 High-frequency amplification

Figure 49 shows a 450 MHz amplifier stage using a neutralized 2N5397. Here the feedback path incorporates a 40 pF capacitor to ensure d.c. isolation between

the gate and the drain, and the neutralizing inductance is varied by adjustment of an aluminium slug inside the ceramic former.

Both the input and output circuits are capacitively tuned, and at the input the inter-electrode capacitance contributes significantly to the tuned network.

The practical difficulties involved with neutralization should not be minimized, for each circuit must be carefully adjusted for maximum gain at the desired frequency, a procedure clearly making for an increased production cost. Further, if a.g.c. is used, the resulting changes in the operating point of the FET will result in a variation in the value of C_{gd} , so that optimum neutralization cannot be maintained. However, it should be kept in mind that a FET stage is much less critical in this respect than is a bipolar stage.

The dotted line of Figure 49 represents the shielding which must exist between the gate and drain leads for minimization of spurious feedback. The actual layout of this shielding in relation to other components is quite critical, and is usually optimized by trial and error.

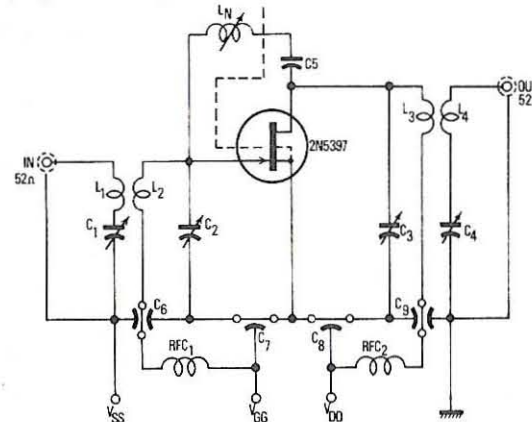


Figure 49 450 MHz neutralized CS amplifier stage¹⁴.

- C1-4 — 0.8-12pF Johanson type 2950
- C5 — 40pF DM5 silver mica
- C6-9 — 1000pF Allen-Bradley type FA5C
- L1 — 1.4" long; 22 gauge enamel, spaced 0.1" from L2
- L2 — 1.1" long; 16 gauge solid copper
- L3 — 1.3" long; 16 gauge solid copper
- L4 — 1.4" long; 22 gauge enamel, spaced 0.3" from L3
- RFC1,2 — 0.15 μ H Delevan type 1537-00
- LN — 3 turns 22 gauge enamel, 0.25" ceramic former; aluminium slug

The common-gate circuit, not having a frequency-dependent neutralization path, is not only free from the relevant adjustment problems, but is effective as a wider band amplifier. It does, however, exhibit a lower power gain than does the equivalent CS stage.

Though the low value of C_{ds} makes the CG stage eminently suitable as a high frequency amplifier in principle, the shielding problem remains a critical one. For example, in the circuit shown in Figure 50, the shielding between the input and output (that is, between the source and drain leads) must be such that the stray capacitance is less than about 0.05 pF.

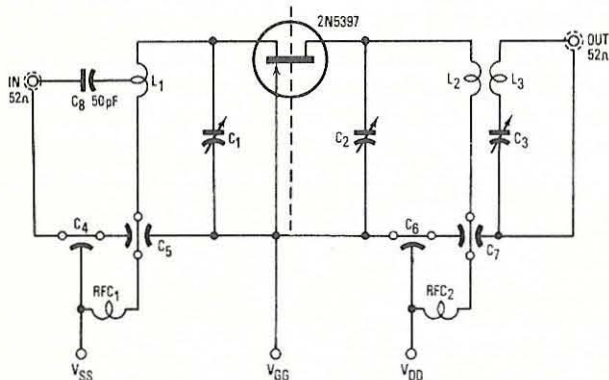


Figure 50 450 MHz CG amplifier stage¹⁴.

- C1-3 — 0.8-12pF Johanson type 2950
- C4-7 — 1000pF Allen-Bradley type SS5D
- RFC1,2 — 0.15 μ H Delevan type 1537-00
- L1 — 1.5" long, 16 gauge copper
- L2 — 1.2" long; 16 gauge copper
- L3 — 2.0" long; 22 gauge copper enamel, loosely coupled to L2, 0.75" spacing

An alternative to neutralization in a CS stage is to employ the cascode connection¹⁵. The basic circuit is shown in Figure 51, from which it can be seen that a CS stage has a CG stage acting as its load. This means that a very low load is presented to the CS stage, so that its voltage gain — and hence its Miller capacitance — is small. It also produces power gain, and the CG stage produces voltage gain, so that the overall result is comparable to that of a neutralized CS stage. The cascode connection removes the necessity for a neutralizing inductance, and makes possible an amplifier having good bandwidth.

The y-parameters for the composite cascode stage may be obtained from the CS y-parameters, and upon making the relevant calculations it is found that the only

value which is strikingly different from the comparable CS values is that of the reverse transmittance, y_{rc} . This is the parameter which describes the capacitive feedback path within the cascode stage, and for two similar FET's this capacitance is:

$$C_{(g1 - d2)} \simeq C_{gd} \frac{g_{os}}{g_{fs}} \quad \dots (5.4)$$

Clearly, to make $C_{(g1 - d2)}$ as small as possible, a FET with a low g_{os}/g_{fs} ratio should be selected.

Figure 51 Basic cascode configuration.

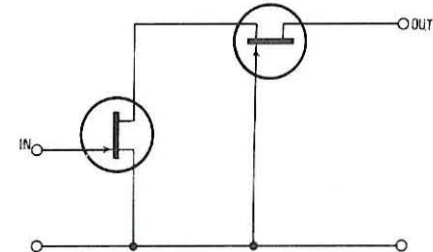


Figure 52 gives a circuit for a cascode stage using two Siliconix U183 FET's, which are low-cost industrial N-channel types. This circuit may be tuned to work up to almost 100 MHz, and though its gain is inferior to the equivalent circuit using a single higher-frequency FET, the two U183 FET's taken together are distinctly cheaper.

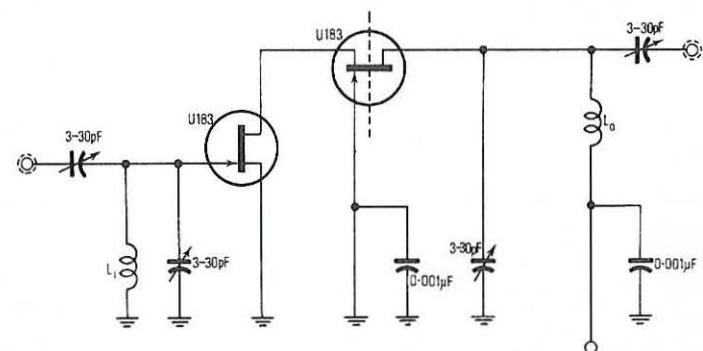


Figure 52 Cascode amplifier for 40-80 MHz

- L_i — tune with 30pF
- L_o — tune with 20pF

Summarizing, it may be said that for stages operating up to about 200 MHz, the cascode stage should be investigated as possibly the cheapest solution; for high power-gain stages up to 500 MHz, the neutralized CS stage is likely to be preferred

while for less critical, but lower gain stages, the CG configuration is most suitable. Where frequencies higher than 600 MHz are involved, use of the flip-chip FET becomes mandatory.

5.6 Stability at high frequencies

As a feedback path exists from the output to the input of a FET stage (C_{gd} for the CS configuration), the admittance at the input is in part a function of the admittance at the output. This internal feedback is taken into account in the y-parameter circuit by the current generator, $y_r E_{out}$. If the output load consists of a tuned circuit, as is usual, then at frequencies above resonance the admittance at the output ($Y_L + y_o$) will be inductive. A calculation based upon this fact will show that within some band of frequencies, the admittance at the input will turn out to have a negative real part. This means that for some values of input generator impedance, frequencies may exist such that the total admittance at the input becomes zero; so that oscillations can be sustained at these frequencies. If it is desired to operate the amplifier with a tuned input circuit, this condition for oscillation is quite likely to be met, and it therefore becomes necessary to modify the simple initial design so that the real part of the admittance at the input remains positive.

Linville and Gibbons* have used this concept to obtain expressions which will predict whether a stage will be unconditionally stable. They define a power gain as:

$$G_{oo} = \frac{|y_f|^2}{4g_i g_o - 2\text{Re}(y_f y_r)} \quad \dots (5.5)$$

where g_i and g_o are the real parts of y_i and y_o (the remaining subscripts have been omitted because the technique is valid for the CS, CG, cascode or any other connection for which four-pole admittance parameters are known). Also, $|y_f|$ is the modulus of y_f ; and $\text{Re}(y_f y_r)$ is the real part of the product $y_f y_r$. Then a stability factor C is calculated:

$$C = 2G_{oo} \left| \frac{y_r}{y_f} \right| \quad \dots (5.6)$$

where

$$\left| \frac{y_r}{y_f} \right| \text{ is the modulus of the quotient } y_r/y_f.$$

If C is less than unity and G_{oo} has a positive value, the circuit is unconditionally stable, and G_{oo} is within 3 dB of the maximum possible power gain, which is:

$$G_{(max)} = \frac{2G_{oo} [1 - \sqrt{1-C^2}]}{C^2} \quad \dots (5.7)$$

* Linville & Gibbons, "Transistors and Active Circuits", McGraw-Hill 1961.

The two expressions (5.5) and (5.6) may be combined to give a single stability criterion, which is that:

$$\left[g_i - \frac{\text{Re}(y_r y_f)}{2g_o} - \frac{|y_r y_f|}{2g_o} \right] > 0 \quad \dots (5.8)$$

Gosling[†] has pointed out that for a simple CS stage, g_i is essentially zero (until the frequency becomes so high as to be limited by circuit practicalities), so that inequality (5.8) cannot be met. However, if the inequality is re-written to include generator and load conductances*, g_G and g_L , it becomes:

$$\left[(g_G + g_i) - \frac{\text{Re}(y_f y_r)}{2(g_o + g_L)} - \frac{|y_r y_f|}{2(g_o + g_L)} \right] > 0 \quad \dots (5.9)$$

It is now possible to choose external components so that stability is achieved. Gosling also shows that this procedure is equivalent to reducing the gain of the stage at the frequency of interest, and in the present text, this can be seen by returning to expressions (5.5) and (5.6). Suppose that the power gain, G_{oo} , turns out to have a positive value, but that C proves to be greater than unity. As G_{oo} is present in the numerator of C, it is clearly necessary only to reduce its value until C falls below unity. This is most easily done by shunting the output with a conductance which will be additive with g_o , and which will be large enough to reduce G_{oo} by the amount necessary to bring C below unity. This reduced value of G_{oo} may then be inserted into equation (5.7) to determine the actual power gain for the stage.

The CG stage will normally give a positive value for G_{oo} , and C will be less than unity. This is because g_i is large if compared to the CS connection, as can be seen from Figure 48, page 77. This does not mean, however, that the practical stage is always stable, for the problems of stray capacitance still exist.

Stability can be obtained by perfectly neutralizing a CS stage, though this is a very difficult task in practice. For such a stage, equations (5.2a) show that no reverse transadmittance exists, so that the stability factor C is zero and the stage is inherently stable. The value of G_{oo} is now:

$$G_{oo}(CSN) = \frac{|y_{fs} - y_{rs}|^2}{4(g_{is} + g_{rs})(g_{os} + g_{rs})} \quad \dots (5.10)$$

which is the maximum power gain, $G_{(max)}$, because as $C \rightarrow 0$, the expression for $G_{(max)}$ in equation (5.7) tends to G_{oo} .

5.7 Power gain

Searle et al** also derive the following y-parameter expression for the power gain in the case of a mismatched two-port network by taking the load admittance

[†] Gosling, Townsend and Watson, "Field-Effect Transistors", Butterworth Group, 1970

* Searle et al, "Elementary Circuit Properties of Transistors", Wiley (1964), pp 249-251

** loc.cit.

Y_L into account:

$$A_P = \frac{|y_f|^2 R_e(Y_L)}{|y_o + Y_L|^2 R_e(y_i + Y_1)} \quad \dots (5.11)$$

where

$$Y_1 = -\frac{y_f y_r}{y_o + Y_L}$$

This expression is difficult to solve when the load is a tuned circuit, because Y_L will be an increasingly marked function of frequency as resonance is approached. However, for a unilateralized CS stage, or for a CG stage, where the reverse transfer y -parameter can be taken as essentially zero, Y_1 also becomes zero. Equation (5.11) can thus be simplified for the resonance condition as follows:

$$A_P(\text{resonance}) = \frac{|y_f|^2 G_L}{g_i(g_o + G_L)^2} \quad \dots (5.12)$$

For the maximum power transfer condition, where $G_L = g_o$, this becomes:

$$A_P(\text{max})(\text{resonance}) = \frac{|y_f|^2}{4g_o g_i} \quad \dots (5.13)$$

This equation does, of course, imply that the two-port is conjugate terminated, which is the condition necessary for the derivation of the Linvill power gain, G_{OO} . Hence, for the unilateralized CS stage, it is identical with equation (5.10) where the composite y -parameters for the unilateral network are substituted (see equations 5.2).

As an example, let the CG y -parameters for the 2N5397 be substituted in equation 5.12. These are (from Figure 48, page 77):

$$y_{ig} \simeq 7.2 + j5.2$$

$$y_{fg} \simeq -8.0 - j0.9$$

$$y_{og} \simeq 0.13 + j5.0$$

$$y_{rg} \simeq -0.2 - j0.3$$

so that

$$A_P(\text{max})(\text{resonance}) \simeq \frac{|64 - 0.81|}{4 \times 0.13 \times 7.2} = 17 \quad \text{or } 12.3 \text{ dB}$$

This is the maximum power gain possible from a properly designed circuit such as that of Figure 50, page 77 .

5.8 Noise consideration

When a FET operates at high frequencies, the noise current generator is likely to be dominant; as would be expected having regard to Figure 31 , page 54 where \bar{e}_n is seen to become constant and low, whilst \bar{i}_n continues to rise. This situation arises mainly because of noise transmission through inter-electrode capacitances, which results in the two input noise generators becoming partly correlated at high frequencies. An approximate expression for the noise current generator is:

$$\bar{i}_n \simeq \sqrt{2qI_{GSS}} + \frac{\bar{e}_n}{X_{C_{rss}}}$$

Unfortunately the optimum generator conductance which results in a minimal noise factor* is normally very different from that which results in maximal power transfer. Compton¹⁴ points out that if a multi-stage amplifier is matched for maximum midband power gain, then the noise factors are:

$$NF = 1 + \frac{9G}{g_{fs}} \quad \text{for a CS stage}$$

$$NF = 1 + \frac{1}{1 + \frac{g_{fs}}{9G}} \quad \text{for a CG stage.}$$

which indicates that for low noise performance it is desirable that the conductance of the generator should be small.

5.9 The FET mixer

A mixer circuit accepts a h.f. modulated input signal, mixes it with a h.f. unmodulated signal derived from a local oscillator, and produces a series of frequencies which are functions of the original two. One of these, the difference frequency, is selected by tuned circuits, and is referred to as the intermediate frequency, or IF. The IF, which is modulated with the same waveform as the incoming signal, is then amplified and the modulating signal extracted for use. The purpose of this system is to produce a signal lower in frequency than the incoming signal so that it may be handled more effectively (and more cheaply).

Normally, the input signal, v_A , is injected at the gate of the FET, and this input circuit is tuned to resonate at the frequency f_A . The local oscillator signal, v_B , may be injected either at the gate or the source. The output signal is tuned by the output circuit so that frequency components other than $(f_A - f_B)$ are much attenuated.

That mixing occurs at all is dependent upon the non-linearity of the transcon-

* see Van der Ziel, "Solid State Physical Electronics", Prentice-Hall 1967

ductance curve; that is, the fact that g_{fs} is a function of the drain current i_D . Normally the local oscillator voltage $v_B (= V_B \sin \omega_B t)$ is large, and is injected either at the gate or the source so that the value of g_{fs} is dependent on it. Then the (small) modulated input signal v_A is injected at the gate, so that i_D becomes a function of both. That is:

$$i_D = f(g_{fs}, v_A) \\ = f'(v_B, v_A)$$

A large signal analysis of this situation shows that optimum conversion transconductance ($g_c = di_D(i_F)/dv_A$) occurs for either of two bias conditions:

(i) $V_{GSQ} \approx V_P$

Here V_B can be made nearly equal to V_P , so that only one half of the local oscillator waveform is actually used for g_{fs} control.

(ii) $V_{GSQ} \approx \frac{1}{2}V_P$

Here $V_B \approx \frac{1}{2}V_P$, and the full waveform is used for g_{fs} control.

In both cases the theoretical value of g_c turns out to be $\frac{1}{4}g_{fs0}$, but as the curvature of the transconductance curve departs markedly from a square-law at low values of i_D , g_c for the $V_{GSQ} \approx V_P$ case is actually poorer than predicted. This is further aggravated by the harmonics resulting from the fact that only half of the v_B waveform is used under these circumstances.

The conversion voltage gain of the mixer is given simply by:

$$A_{vc} \approx g_c Z_L$$

where Z_L is the load impedance.

A typical mixer circuit using gate injection is given in Figure 53.

5.10 Cross modulation

If two signals enter an amplifier stage, one of which is modulated, then the other signal becomes modulated to some extent in its passage through the stage. This is termed cross-modulation. For a wide-band h.f. stage this can be serious, but for a tuned stage it is usually unimportant.

In the case of a mixer, it may turn out that the IF output signal has become modulated not only by the wanted modulation, but also by some unwanted modulation which may be present upon another, arbitrary, input signal.

Cross modulation for the amplifier and the mixer is a result of departures of the transconductance curve from a true square law. For an amplifier the third-order terms relevant to this curve produce cross-modulation, and for the mixer

the fourth-order terms result in cross-modulation observed at the intermediate frequency. The fact that the transconductance curve of the FET is closer to a pure square law than that for any other device, however, does make it clear that its performance in h.f. circuits is likely to be much superior to that of the bipolar transistor in this context.

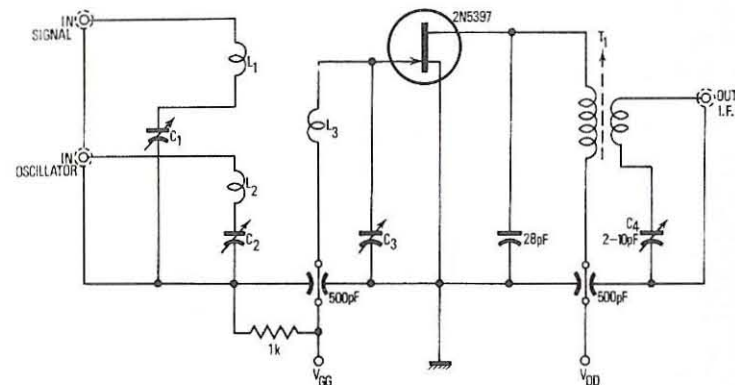


Figure 53 A gate-injection mixer stage

- C1-4 — 0.8-12pF Johanson type 2950
- L1 — 1.4" long; 22 gauge enamel, close coupled to L3
- L2 — 1.6" long; 22 gauge enamel, close coupled to L3
- L3 — 1.75" long; 16 gauge copper
- T1 — Primary: 13 turns, 22 gauge enamel, close wound on 0.25" former approx. 1μH
Secondary: 3 turns, 22 gauge enamel, close wound over primary

FET SWITCHES, CHOPPERS AND ANALOG GATES

6.1 The FET as a switch

Dependent upon the value of V_{GS} , the channel of a FET working well below saturation can present a wide range of (nearly) ohmic resistance. This has already been discussed in Chapter 4, and typical values of r_{DS} for some P-channel FET's were shown in Figure 12, page 23. From this diagram it is apparent that the FET channel can be considered to represent a switching element; while V_{GS} represents a switch-controlling voltage.

For a FET switch, three primary factors are of immediate interest:

(i) The ratio of OFF to ON resistance

When $V_{GS} = 0$, the channel of a junction FET presents a minimal resistance $r_{DS(on)}$. This can be very small: for example, the Siliconix 2N5432 has a guaranteed maximum $r_{DS(on)}$ of only 5 ohms. Insulated gate FET's (MOSFET's) normally have a somewhat higher $r_{DS(on)}$, but in the case of the Siliconix 3N167 P-channel enhancement MOSFET, this is typically only 20 ohms at $I_D = 0.1$ mA. In both cases the fully pinched-off channels represent very large resistance indeed, and $I_{D(off)}$ is in fact the leakage current between drain and gate (or between drain and substrate for a MOSFET).

For the 2N5432, $I_{D(off)} = 200$ pA at $V_{DS} = 5$ volts
and $V_{GS} = -10$ volts
and for the 3N167, $I_{D(off)} = 500$ pA at $V_{DS} = -20$ volts
and $V_{GS} = 0$

Although the existence of $I_{D(off)}$ (and $I_{S(off)}$) make a true measurement difficult, the channel OFF resistance can be assumed to approach 10^{12} ohms. The voltage drop across the channel during the ON condition is given by:

$$V_{DS(on)} = \frac{V_{DD} r_{DS(on)}}{R_D + r_{DS(on)}} \quad \dots (6.1)$$

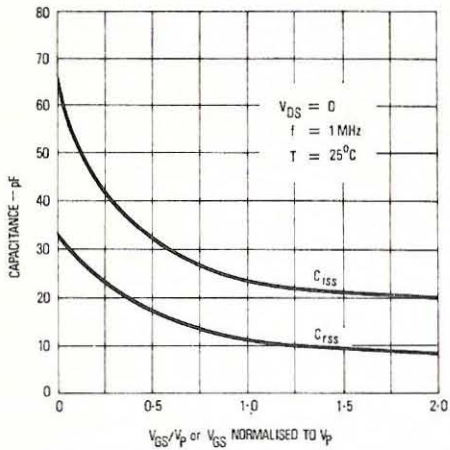
and during the OFF time by:

$$V_{DS(off)} = V_{DD} - I_{D(off)} R_D \quad \dots (6.2)$$

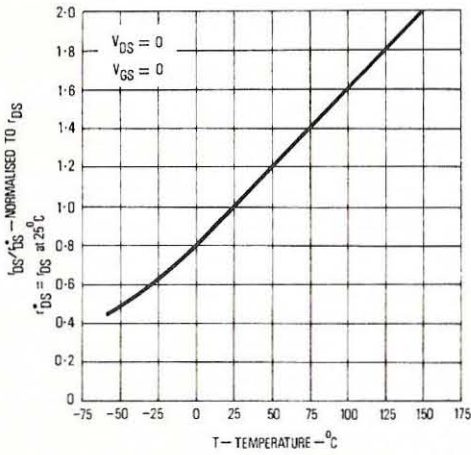
Figure 54 (in which some characteristics for the Siliconix 2N5432 are reproduced) shows how $r_{DS(on)}$ and $I_{D(off)}$ vary with temperature. As would be expected of a silicon device, the channel resistivity increases with temperature, so that $r_{DS(on)}$ rises; and because $I_{D(off)}$ is largely the drain-gate leakage current, this also rises with temperature, as is shown in diagram

(c). These known variations enable equations 6.1 and 6.2 to be used in designs where a range of operating temperatures must be taken into account.

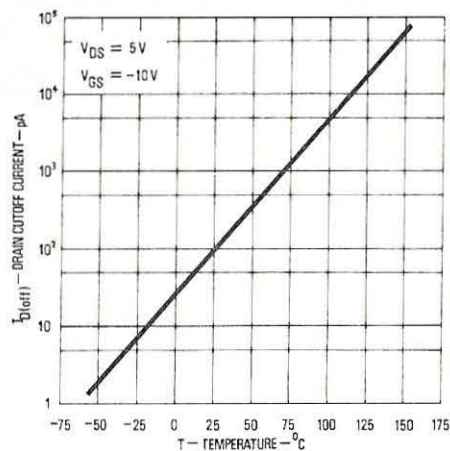
Figure 54 Characteristics of the Siliconix 2N5432 series switching FET's.



(a) inter-electrode capacitances versus gate voltage (normalized to V_p)



(b) drain-source resistance versus temperature (normalized to 25°C).



(c) $I_D(\text{off})$ versus temperature.

From the foregoing discussion it is clear that the FET can in principle perform all the switching functions of the bipolar transistor. There are, however, some disadvantages; including somewhat lower switching speed, and the fact that V_p must by definition be greater than V_{BE} . It is good design practice therefore to utilize the FET for switching circuits in which its *unique* properties may be put to use. Figure 55 gives a series of sketches showing channel resistance variation with V_{GS} for the family of six field effect devices. These diagrams indicate that any desired rise or fall in channel resistance can be produced for a given drive signal by correct choice of field effect device; provided, of course, that the magnitude of the drive signal is greater than V_p or $V_{GS(th)}$.

(ii) The offset voltage

If a bipolar transistor is used as a switch, a base current must flow when the device is in the ON condition. Thus the emitter-collector path is 'active' under these circumstances, so that a small voltage $V_{CE(\text{offset})}$ always appears across an ON bipolar transistor. Even the best bipolar devices present an offset voltage of the order of a millivolt. By comparison, the FET presents zero offset voltage, which is evident from Figure 12a, page 22 where all the characteristics can be seen to pass through the origin. This property is particularly advantageous when choppers for low-level d.c. amplifiers are to be designed (as will be seen later).

(iii) Switching speed

The time taken for a FET to switch ON and OFF is determined by both the external circuitry and the inter-electrode capacitances, along with the

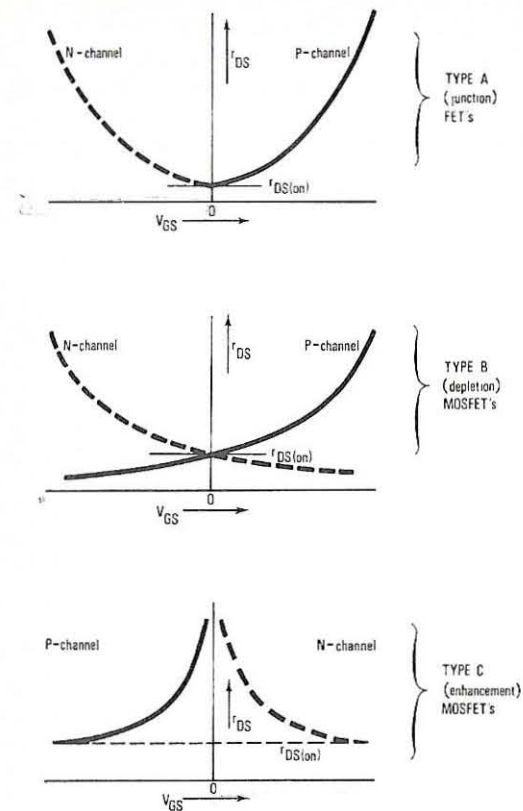


Figure 55 Channel resistance versus gate voltage characteristics.

channel resistance. For fast switching times it is sensible to select a FET with low inter-electrode capacitances, but as this implies a small-geometry device, the value of $r_{DS(on)}$ is likely to be high. The following table illustrates the form of compromise which must be drawn between these capacitances and $r_{DS(on)}$:

Device	$r_{DS(on)} (max)$	$C_{iss}(max)$	$C_{rss}(max)$
2N5432	5 ohms	30 pF	15 pF
2N4091	30 ohms	16 pF	5 pF
2N3824	250 ohms	6 pF	3 pF

Switching speed is conveniently defined for a specific circuit configuration in Figure 56 (b). Here a square-wave having a very fast rise-time and fall-

time is applied to the gate, and a set of switching times relevant to the channel is defined as:

t_d = turn-ON delay time (the time taken for I_D to rise to 10% of its maximum value)

t_r = rise time (the time for I_D to rise from 10% to 90% of its maximum value)

t_{off} = turn OFF time (the time for I_D to fall to 90% of its maximum value)

t_f = fall-time (time for I_D to fall from 90% to 10% of its maximum value)

These definitions are further illustrated in Figure 56 (a). Actual values for switching times, along with measurement conditions, are given for the Siliconix 2N5432 series in Figure 56 (b) as examples of the magnitudes to be expected.

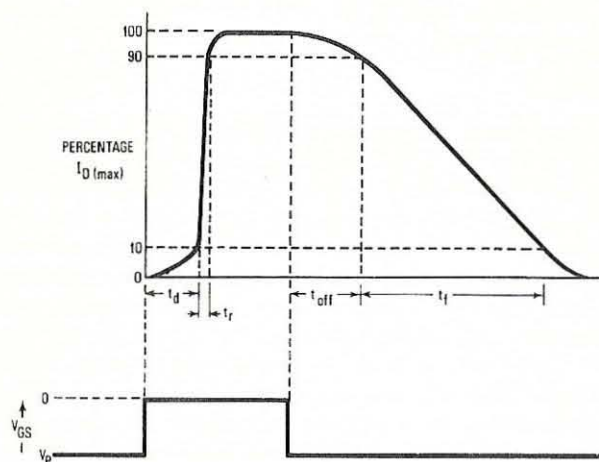


Figure 56a Switching time definitions

Characteristic	Test conditions	Each device		Unit
		min	max	
t_d Turn-ON delay time	$V_{DD} = 1.5$ volts		4	ns
t_r Rise time	$V_{GS(ON)} = 0$		1	ns
t_{off} Turn-OFF time	$V_{GS(OFF)} = -12$ volts		6	ns
t_f Fall time	$I_{D(ON)} = 10$ mA		30	ns

INPUT PULSE
rise time 0.25 ns
fall time 0.75 ns
pulse width 200 ns
pulse rate 550 pps

SAMPLING SCOPE
rise time 0.4 ns
input resistance 10 M Ω
input capacitance 15 pF

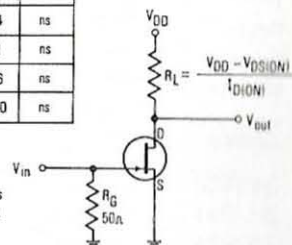


Figure 56b Switching times for the Siliconix 2N5432

The inter-electrode capacitances C_{iss} and C_{rss} are essentially components of the distributed junction capacitance, and as such are inverse functions of the depth of the depletion layer — which in turn is a function of the gate-channel voltage. Consequently both C_{iss} and C_{rss} vary with the reciprocal of V_{GS} , as shown in Fig. 54(a), which means that accurate calculation of switching speed is rendered difficult due to these variations.

However, because the FET is a majority-carrier device, and so does not exhibit minority-carrier storage phenomena (as does a bipolar transistor), the interelectrode capacitances can have a dominating effect upon its transient performance. That is, the interelectrode capacitances affect not only switching speed, and hence the bandwidth of the circuit, but will also allow some capacitive feedthrough of the gate drive waveform. These effects may be considered in a simplified empirical manner when related to specific switching configurations, such as the chopper and analog gate (Sections 6.2 and 6.3).

The wide range of I_{DSS} values available (up to 0.3 ampere min. for the Siliconix U244 10-watt power FET) makes it possible to use FET switches for almost any purpose, from low-level logic to small power switching. There are also certain unique properties which make some members of the family extra valuable for specific applications. For example, the fact that the P-channel enhancement MOSFET requires a gate voltage polarity of the same sense as the drain voltage means that it may be directly coupled to other, similar, MOSFET's to perform logic functions with very simple circuit configurations. This property, together with ease of fabrication, has made it the standard element for medium and large scale integrated circuits (MSI and LSI).

Also the fact that the FET exhibits zero offset voltage has led to its very widespread use in chopper amplifiers and as an analog gate. These two important applications are now considered further.

6.2 The FET chopper

The block diagram for a d.c. amplifier using an electro-mechanical chopper was given in Figure 45, page 70. Such an amplifier is, in fact, very successful in that drift levels can be made very low indeed (better than $0.1 \mu V/^\circ C$): but the system suffers from the disadvantages of finite chopper life and a chopping frequency limited by mechanical considerations. Bipolar transistors can replace the electro-mechanical chopper, and will solve the problems of life and chopping frequency most successfully: they do, however, introduce other problems. Paramount is the severe limitation on smallness of signal which can be amplified, resulting from the existence of the offset voltage between emitter and collector in the ON condition. Also, the ratio of OFF to ON resistance is much poorer than for an electro-mechanical chopper; and this is even worse for the photo-chopper, which is a photoconductive cell illuminated by a square-wave of light flux.

As the FET presents no offset voltage*, it is particularly useful as a modulator for chopper-type d.c. amplifiers¹⁶, though the form taken by the demodulator is less important as the output signal is usually large. Figure 57 shows two FET's connected as the modulator and demodulator of a chopper-type d.c. amplifier, driven in anti-phase so as to simulate the action of the double-pole electro-mechanical chopper.

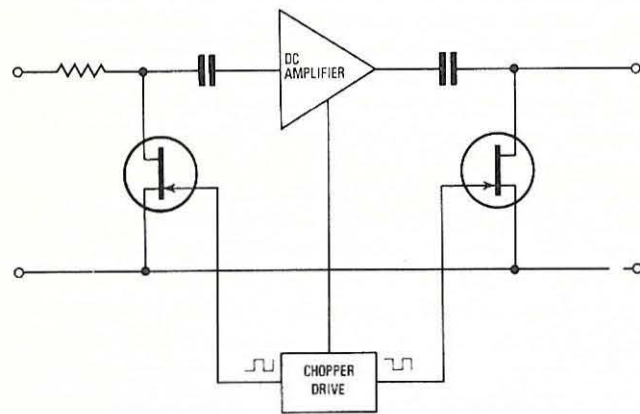


Figure 57 DC amplifier using FET choppers

These FET's are connected as shunt choppers, and Figure 58 (a) details the input chopper circuit; diagrams (b) and (c) giving equivalent circuits for ON and OFF conditions respectively.

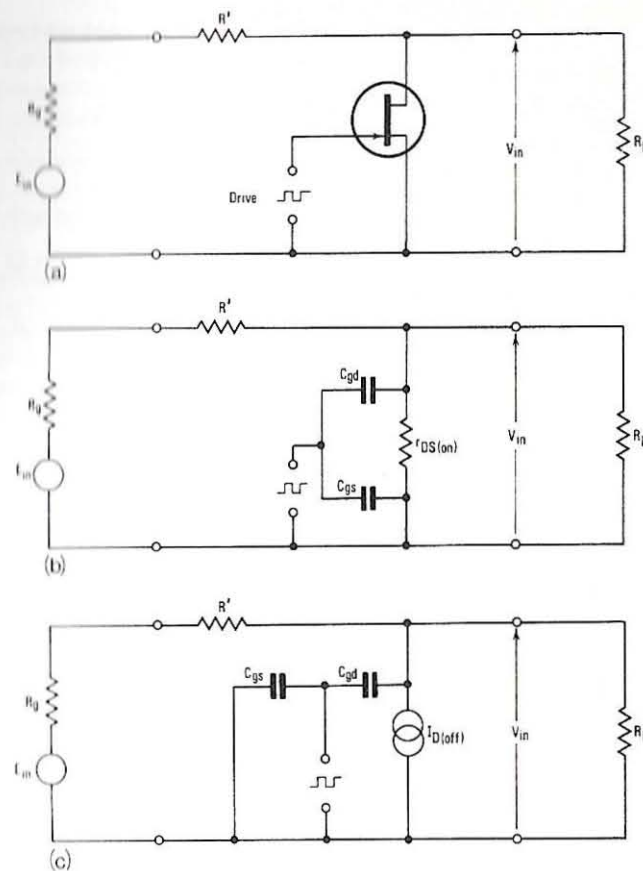


Figure 58 (a) The FET shunt chopper
(b) The ON state equivalent
(c) The OFF state equivalent

The (normally very small) generator voltage is E_{in} , and when the FET is ON the voltage presented to the amplifier is ideally zero, but in practice given by:

$$V_{in} = \frac{E_{in} R^*}{R_g + R' + R^*} \quad \dots (6.3)$$

where

R_g is the internal resistance of the input voltage generator

R' is any other resistance in series with the input

and

R^* is the parallel combination of $r_{DS(on)}$ and R_L .

* Offsets do appear as a result of switching transient breakthrough and thermal e.m.f.'s — the latter rarely exceeding a few microvolts. Transient breakthrough will be considered later.

As the input resistance to the amplifier, R_L , is normally very much larger than $r_{DS(on)}$, equation 6.3 reduces to:

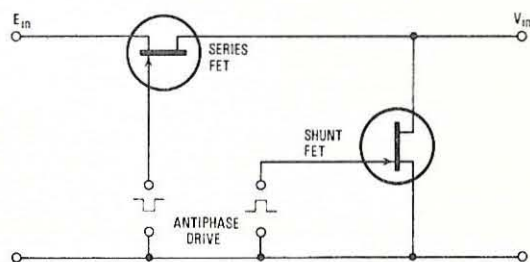
$$V_{in} = \frac{E_{in} r_{DS(on)}}{R_g + R' + r_{DS(on)}} \quad \dots (6.4)$$

During the OFF conditions (and also because R_L is very large),

$$V_{in} = E_{in} - I_{D(OFF)} (R_g + R') \quad \dots (6.5)$$

For optimum operation, V_{in} during the ON condition should obviously be as small as possible. Equation 6.4 suggests that to attain this $(R_g + R')$ should be as large as possible. However, equally obviously V_{in} should closely approach E_{in} during the OFF condition, which suggests that $I_{D(off)}$ and $(R_g + R')$ should both be as small as possible! To choose a FET with a very low $I_{D(off)}$ is reasonable, but the resolution of the conflicting requirements in $(R_g + R')$ must remain dependent upon the numerical values obtained from equations 6.4 and 6.5. Usually a compromise solution is adequate: if not, a more complex chopper may be utilized — such as the shunt-series configuration of Figure 59.

Figure 59 *The series/shunt FET chopper*



Here a series FET replaces R' and is driven in antiphase compared with the shunt FET. Consequently, when the shunt FET is ON, the series FET is OFF, so that R' is very large indeed. Conversely, when the shunt FET is OFF, the series FET is ON, so that R' is now very small. Hence equations 6.4 and 6.5 are both optimized by this technique.

Note that if complementary FET's are used (that is, one N and one P-channel type), antiphase drives are not required. However, because a multivibrator is usually used as a drive generator, signals in antiphase are normally available. Further, it is much cheaper to use matched FET's of one polarity than to attempt to match complementary pairs. This is because the question of matching in this context includes similarity of switching times, and hence inter-electrode

capacitances, for it is clearly necessary to ensure that any interval when the FET's are both ON or both OFF should be extremely short. The stringency of these requirements does in fact make the satisfactory matching of complementary pairs almost impossible.

Inter-electrode capacitances are also important from the viewpoint of switching signal feedthrough, leading to the appearance of transient spikes superimposed on V_{in} . The nature of these spikes is apparent from a consideration of Figure 58 (b) and (c). When the FET is switched OFF from the ON condition, the negative-going leading edge of the switching waveform generates a transient current which divides between C_{gs} and C_{gd} . The former component is taken to ground, but the latter passes through C_{gd} to the signal circuit and produces a voltage drop across R_L in parallel with $(R' + R_g)$ and r_{ds} . If the FET has switched hard OFF, r_{ds} will be large, and as R_L is also large, the height of the spike will be determined mainly by $(R_g + R')$.

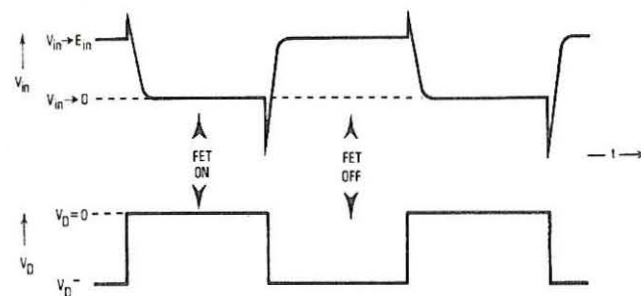


Figure 60 *Shunt N-channel FET chopper waveforms.*

Figure 60 shows this negative-going spike superimposed upon V_{in} . When the FET switches from OFF to ON, the positive-going trailing edge produces a voltage transient in the opposite direction. This will, however, be smaller than the negative-going transient because the FET now presents a low value of r_{ds} ($=r_{DS(on)}$ when hard ON), and this reduces the voltage drop considerably. This transient is also shown in Figure 60.

The *average* value of these transients appears as a small apparent offset voltage. For very low-level applications, therefore, a FET having very low inter-electrode capacitances should be chosen, even though $r_{DS(on)}$ will inevitably be higher. Also, the series-shunt configuration should be considered seriously; it does result in a diminution of transient spikes, owing to the changing resistance presented by each FET to the other during switching.

Whatever the choice of drive circuit, care should be taken to establish that $|V_p|$ for the chopper FET's is exceeded during their OFF states so that signal breakthrough cannot occur. Note that if the signal polarities demand the use of

P-channel FET's, the foregoing discussion still applies, but that it is more difficult to effect a good compromise between a low $r_{DS(on)}$ and low inter-electrode capacitances.

This follows from the fact that, owing to the lower mobility of holes compared with electrons, the channel resistance of P-type FET's in general is higher than that for N-types. P-channel devices are rarely required, however, because E_{in} is normally very small. Thus the N-channel FET can be considered fully bilateral.

The question of applying the correct drive to the series FET is most conveniently considered in the context of analog gates, which are now to be discussed.

6.3 The analog gate

The analog gate is essentially a switch which can either be cut off, or will allow the (undistorted) passage of a time-varying signal. Because mechanical switches are comparatively slow and have limited lives — even the reed relay, which is the most successful switch to date — the FET has achieved considerable popularity in this application¹⁷

Fundamentally, the FET analog gate is a series-connected switch, as shown in Figure 61. It is driven by a sampling waveform which for the N-channel device shown, consists of a direct voltage greater than $|V_p|$ which rises to zero each time E_{in} is to be sampled. Frequently a number of channels need to be sampled consecutively and then applied to a single processor (e.g. an amplifier and recorder): such a system is shown in Figure 62. This is usually called a commutator, or multiplexer, which, because it consists of a number of identical FET's, is peculiarly suited to fabrication as an integrated circuit. These will be discussed in the next Chapter; for the present it is necessary to consider further the simple circuit of Figure 61.

The sampled signal to the load, R_L , will be, for the ON condition of the FET:

$$V_{in} \approx \frac{E_{in} R_L}{R_g + r_{DS(on)} + R_L} \quad \dots (6.6)$$

whereas for the OFF condition of the FET, it will be essentially zero.

In equation 6.6 there are reservations to be made regarding some of the numerical values. Unlike the case for the chopper, E_{in} may not necessarily be small; nor R_L very large: which means that the channel resistance $r_{DS(on)}$ might possibly be operated beyond its limited linear region. Hence some distortion of V_{in} could conceivably occur. That is, the device may operate outside the triode region. Also, if R_L is not very large V_{in}/E_{in} might not approach unity.

The actual value and polarity of E_{in} affects the drive requirements considerably, and the situation may be conveniently summarized by making an inspection of Figure 61.

For the OFF condition, where the FET is essentially an open circuit, E_{in} will

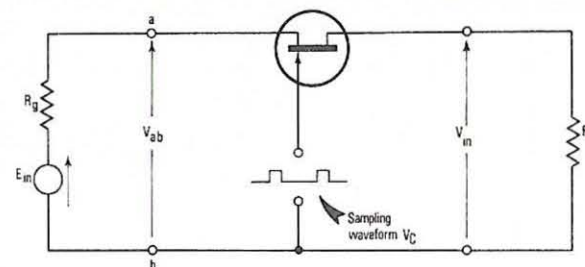


Figure 61 The analog gate

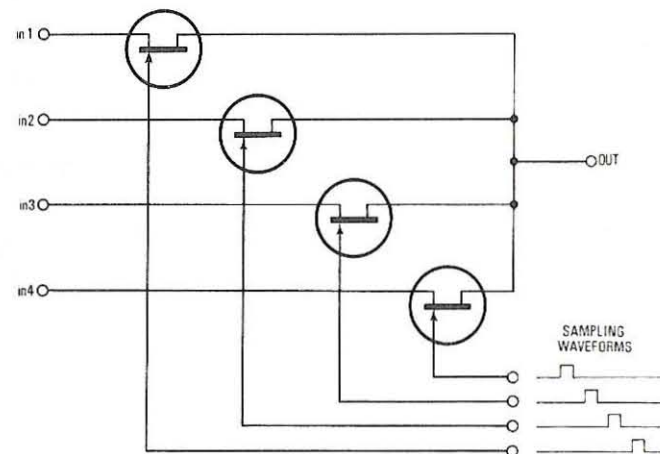


Figure 62 The Commutator or Multiplexer.

appear across points a b there being no voltage drop in R_g . Hence if E_{in} goes negative, it will tend to turn the FET ON again, so that the control voltage, V_C , must be made sufficiently negative to counteract this. That is, if the most negative excursion of E_{in} is E_{in}^- ,

$$|V_{C(off)}| \geq |V_{P(max)}| + |E_{in}^-| + 2 \quad \dots (6.7)$$

Here magnitude signs have been used so that the equation is fully general and applies also to P-channel gates. Also, a rule-of-thumb has been incorporated — that it is useful to exceed the minimum acceptable drive voltage by a safety margin of 2 volts.

Conversely for the ON condition (when V_{GS} should be zero), the FET will tend to be turned OFF if E_{in} goes positive. This means that V_C should go sufficiently positive to counteract this tendency. That is, V_C should go more positive than the voltage which appears across a b:

$$|V_{C(on)}| \geq |V_{ab}^+| \quad \dots (6.8a)$$

where

$$V_{ab}^+ = \frac{E_{in}^+ (r_{DS(on)} + R_L)}{R_g + r_{DS(on)} + R_L}$$

If $R_L \gg r_{DS(on)}$, R_g , this becomes:

$$|V_{C(on)}| \geq |E_{in}^+| \quad \dots (6.8b)$$

If $V_{C(on)}$ complies with this condition, but E_{in} is *below* its maximum positive value of E_{in}^+ , then the junction would be forward-biased. Hence a blocking diode must be inserted as shown in Figure 63. A resistor will effectively tie the gate to the source so that $V_{GS} = 0$ for the ON condition, but will prevent an unacceptably high current from flowing. If desired, a capacitor (shown dotted) may be added so that the switching speed may be increased.

Figure 63 *Analog gate with isolating diode and referencing resistor.*

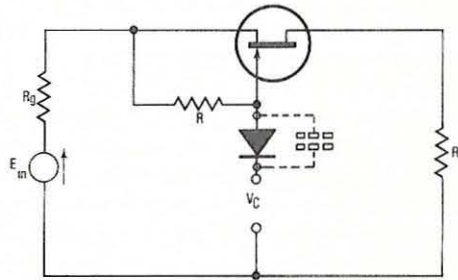
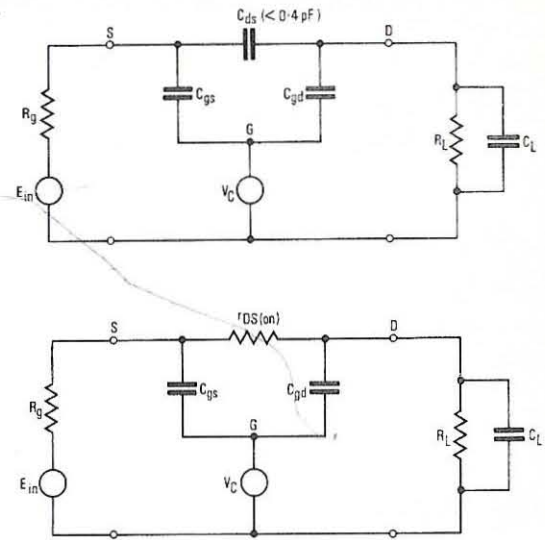


Figure 64 shows the equivalent circuits corresponding to the ON and OFF conditions of the analog switch of Figure 61. When $|V_C|$ rises to turn the FET OFF, r_{DS} also rises until it can be assumed to approximate to an open circuit when $V_{GS} = V_p$. After this, $|V_C|$ continues to rise until the value defined by equation 6.7 is reached, the excess voltage, e_{ov} , above $|V_p|$ being $|V_{C(off)}| - |V_p|$. If V_C has a fast rise time, (much less than $R_L(C_L + C_{gd})$), this excess voltage will divide between C_{gd} and the load capacitance C_L to produce a spike across the load of height e_L , where:

$$e_L \simeq e_{ov} \frac{C_{gd}}{C_{gd} + C_L} \quad \dots (6.9)$$

This spike will decay through the time constant $R_L(C_L + C_{gd})$, and will be repeated for every ON to OFF sequence. If the area under these spikes is averaged per unit time, this will approximate to the apparent offset voltage across the load. Such a calculation will, however, be very approximate, for C_{gd} itself is a function of V_{gd} .

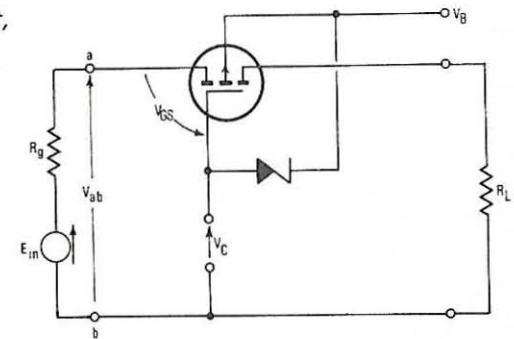
Figure 64 *Equivalent circuits for the FET analog gate; top, OFF condition, lower, ON condition.*



The junction FET can have both a low channel resistance and low inter-electrode capacitances compared to the MOSFET, and is therefore superior in respect of both signal path resistance and switching speed. As has been seen, however, it does require some external circuitry if signals of both polarities are to be accepted, and in this sense is less satisfactory than the MOSFET analog gate.

The basic form taken by the P-channel enhancement MOSFET gate is shown in Figure 65, where it will be seen that a Zener diode structure has been included to protect the insulating layer from overvoltage damage. Some discrete MOSFET's such as the N-channel depletion 2N3136, omit this protective Zener so that they can be used in very low leakage applications.

Figure 65 *Basic analog-switch unit, using P-channel enhancement MOSFET and Zener diode gate protection.*



Recalling that junctions exist between source-substrate and drain-substrate, this substrate (or body) is taken to a supply voltage V_B , whose value is such as to prevent forward-biasing of these junctions under any conditions. That is:

$$V_B \geq E_{in}^+ \quad \dots (6.10a)$$

To prevent forward current flowing through the Zener diode, the substrate voltage must also be greater than the most positive excursion of V_C . That is:

$$V_B \geq V_{C(off)} \quad \dots (6.10b)$$

Hence V_B is defined by the larger of the equations 6.10a or 6.10b.

For the OFF condition, E_{in} appears across points a b, so that should E_{in} go positive, it will be in such a direction as to turn the MOSFET ON if $|E_{in}^+| > |V_{GS(th)}|$. This tendency must be counteracted by V_C , which must therefore go positive by an amount $V_{C(off)}$, where:

$$V_{C(off)} > E_{in}^+ - |V_{GS(th)}(min)| \quad \dots (6.11)$$

Conversely, to turn the MOSFET hard ON, V_{GS} must take a value $V_{GS(on)}$ which is more negative than $V_{GS(th)}$, and which can be extracted from data sheet information. Should E_{in} go negative, it will subtract from $V_{GS(on)}$, so that the (negative) value of $V_{C(on)}$ necessary to ensure that the MOSFET is turned hard ON must be:

$$|V_{C(on)}| \geq |V_{GS(on)}| + |E_{in}^-| \quad \dots (6.12)$$

Having established the swing of V_C , transient considerations can be taken into account in much the same way as for the junction FET switch.

Chapter 7

INTEGRATED CIRCUITS

7.1 Introduction

Modern semiconductor devices are normally fabricated in large numbers on single slices cut from the same crystal of silicon. The planar diffusion process has already been described in terms of a single FET in Chapter 1, and it will be appreciated that several hundred such structures can be made at the same time by using masks printed with suitable matrices of identical patterns.

When the diffusion and passivating processes have been completed, the silicon wafers are scribed in a pattern of squares — each containing one FET structure. Before breaking along the scribed lines the individual 'chips' or 'dice' are tested, and then selected into groups having similar parameters — some being matched to form pairs as explained in Section 4.5.

It is clear that by making interconnections between structures on the same 'dice' a multi-structure or *monolithic integrated circuit* can be produced. The term monolithic here implies that the group of interconnected structures has been formed on one die, as opposed to the multi-chip integrated circuit in which several separate dice are mounted on one header and connected together by external jumper wires.

A third class of integrated circuit consists of structured dice plus discrete components such as chip capacitors; these are termed hybrid integrated circuits. Many hybrid operational amplifiers exist, some combining a dual FET first stage with a bipolar transistor succeeding amplifier, which can itself be either monolithic or discrete.

The fabrication of both field-effect and bipolar structures on a single chip presents technical difficulties, but successful devices have been produced by Siliconix. One, the L120 MOSFET/bipolar amplifier, is described later in the Chapter. Conversely, multiple arrays of switching elements, being easier to fabricate, have proliferated: sundry forms of MSI, LSI and multiple analog-gates are readily available. The latter range of microcircuits has now reached the stage where effective interfaces can be formed between digital and analog networks when associated with the correct drive stages, which themselves can be successfully integrated. These arrays are dealt with in detail in the following sections.

7.2 The multi-channel analog-gate

The discrete array of junction FET's used in commutation and multiplexing, and typified by the four-channel example of Figure 62, page 99, is clearly an excellent candidate for microcircuit fabrication. The Siliconix G125F to G132F

range is a four-channel integrated circuit of precisely this form. The eight members of the range divide into two groups of four, one group with commoned drains (as Figure 62), the other consisting of completely unconnected FET's. The four members of each group have maximum $r_{DS(on)}$ values ranging from 45 to 500 ohms, the two lower resistance devices having somewhat higher inter-electrode capacitances than the two higher.

The four-channel FET switch is a versatile unit, the applications of which include the multiplexer (usually in the commoned-drain version), modulator/demodulator chopper, and the high precision instrument rectifier (along with a sense amplifier). However, care must be taken to avoid the application of signals of too high an amplitude, or of the wrong polarity relevant to the driving systems used, as explained previously in Section 6.3.

The driving problem is simplified if MOSFET rather than junction FET arrays are used¹⁸, because signals of either polarity may be accommodated without the use of the isolating diode or referencing resistor of Figure 63 (page 100). Also, the drive voltage may go both positive and negative, so that greater swings of E_{in} are acceptable; though it should be remembered that if V_{DS} becomes large (i.e. when the channel current is high), non-linearity of the channel resistance will result.

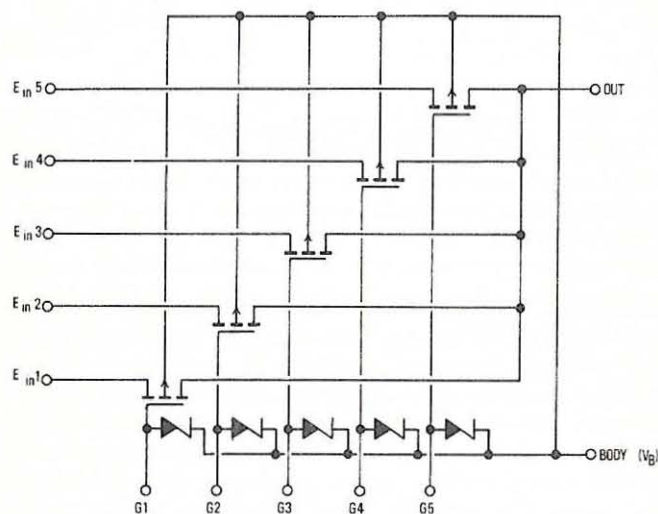


Figure 66 Five-channel MOSFET analog-switch array — e.g. Siliconix G114L

Figure 66 shows an array of five P-channel enhancement MOSFET's corresponding to the Siliconix G114L integrated circuit. Five Zener diodes are also integrated to protect each gate from overvoltages. The positive ends of the Zener diodes are

connected to the substrate or body, which implies that a positive voltage must be applied to the body which is at least equal to the maximum excursion of the control voltage V_C . This is one criterion of operation for the P-channel MOSFET switch. Others may be derived by inspecting the single-channel unit of Figure 65 as was done previously in Section 6.3. As an example of the use of these expressions (6.10 to 6.12), assume that the Siliconix G114L array of Figure 66 is to be run at its maximum allowed voltage of 20 volts peak-to-peak with equal 10 volt excursions about zero. That is, $E_{in}^+ = +10V$ and $E_{in}^- = -10V$.

From the data sheet, $V_{GS(th)}$ is given as lying between -2 and -6 volts, so that inequality 6.11 gives:

$$\begin{aligned} V_{C(off)} &> E_{in}^+ - |V_{GS(th)}| \text{ (min)} \\ &> 10 - 2 = 8 \text{ volts} \end{aligned}$$

Inequality 6.12 is:

$$|V_{C(on)}| \geq |V_{GS(on)}| + |E_{in}^-|$$

Knowing that $V_{GS(on)}$ must be more negative than $V_{GS(th)} \text{ (max)}$, then:

$$\begin{aligned} |V_{C(on)}| &> |V_{GS(th)} \text{ (max)}| + |E_{in}^-| \\ &> 6 + 10 = 16 \text{ volts} \end{aligned}$$

The data sheet states that the excursion of V_C must not exceed 30V, so that it would be reasonable to interpret the numerical inequalities above as giving:

$$V_{C(off)} = +10V$$

and

$$V_{C(on)} = -20V$$

Finally, expression 6.10a gives the body voltage as:

$$V_B \geq E_{in}^+ \text{ which in this case gives } +10V.$$

The switching speed of the array is determined by both the internal capacitance and the rise and fall times of the driving waveform itself. Internal capacitances in MOSFET arrays can be very small — for example, C_{gs} and C_{gd} for the G114L are only 0.5 pF maximum. The source-body and drain-body capacitances are also nominally very small; and are further reduced when the relevant junctions are reverse-biased by a high body voltage V_B . The switching voltage excursions typified by the nominal example given above are easily obtained from other FET or MOSFET circuits, but when the switching array is to be used in conjunction

with bipolar logic — where excursions of a few volts are normal — some design embarrassment may result. For this reason, the question of combining drivers with interfacing networks becomes of importance, and integrated circuits designed to achieve this combination will now be discussed.

7.3 Drivers for field effect switching arrays

The example of the last section indicated that a symmetrical drive voltage of +10V, -20 volts, along with a +10V body voltage was required. This suggests a bipolar driver circuit, having supply rails at +10 and -20 volts. This unit will receive a signal from whatever circuitry is relevant to the design under consideration, but as an example, Figure 67 (a) shows the voltage transfer function of a driver

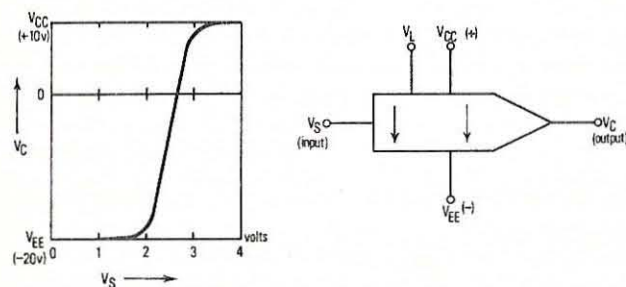
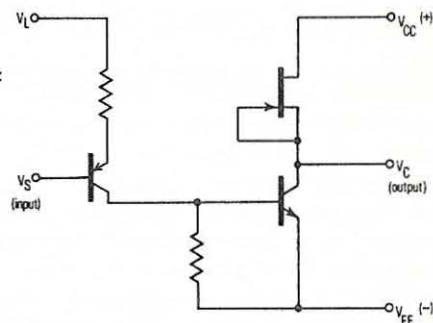


Figure 67 Typical transfer function and symbol for a non-inverting driver unit — e.g. Siliconix D112F or D120F.

intended for use with a 5V positive logic system. Here the output swings to -20V when the input is at zero; and to +10V when the input is at +5V. As both input and output voltages swing in the same direction, the symbol of Figure 67 (b) may be used for this type of driver, a specific example of which is the Siliconix D112F or its faster equivalent, the D120F. These drivers each consist of two of the circuits shown in Figure 68, and operate as follows.

Figure 68 Typical circuit for integrated driver unit — e.g. Siliconix D112F or D120F



When the PNP transistor is ON ($V_S = 0$), the NPN transistor is also driven ON, so that $V_C = V_{EE}$; that is, -20V in the present example. Conversely, when the PNP transistor is OFF ($V_S > V_L$), then $V_C = V_{CC}$, which is +10V in the same example.

Notice that the current to the NPN transistor is supplied not via a resistive load, but via a FET current-limiter, or 'pull-up'. In the case of the D111F to D121F, the pull-ups are integrated along with the other driver elements; but in other cases this is not necessarily so. For instance, the D123F to D125F six-channel drivers do not include pull-ups; instead they are integrated into the relevant analog-gate arrays — the G116F to G119F series. In this case the pull-ups are P-type enhancement MOSFET's, like the analog switches themselves, and they also act as integrated gate protection devices. This is the main reason for including the pull-ups in the switching array rather than the driver, and, in fact, for the G118F the gates of the pull-up MOSFET's are internally connected to the body so that the drain-to-body junctions act as simple protective Zener diodes. Such a connection can be made externally for other members of the range, as is obvious from Figure 69, where the shorting of terminals P and B will produce this result.

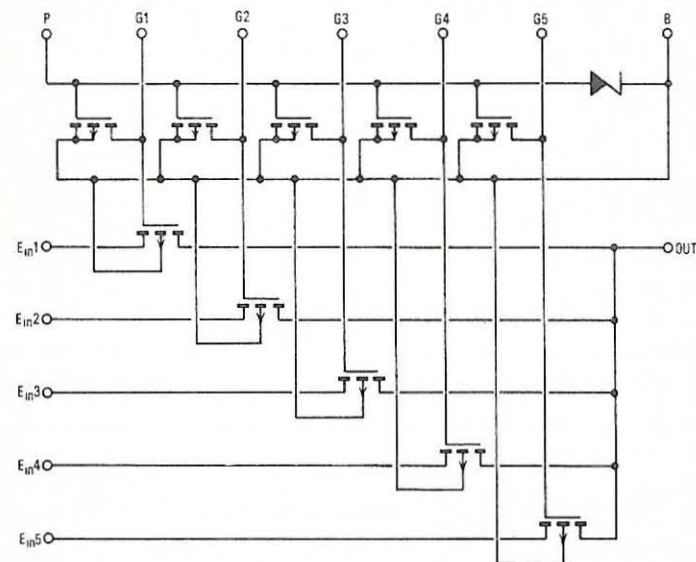


Figure 69 Five-channel analog-switch array with integrated MOSFET pull-ups — e.g. Siliconix G116F

Integrated drivers which will operate from logic voltages below 1.0V are also available, as are drivers which produce internal inversion. For example, a microcircuit which has both of these attributes is the dual driver type D113F

(or D121F), for which a voltage transfer function and symbol are shown in Figure 70.

The switching speed of the driver is governed both by internal and external delays, including the capacitance into which it must operate.

Hence the time delays quoted are relevant to a particular external circuit, and may be augmented by specific increments of time for each extra picofarad of driven capacitance. This convention enables a determination to be made of the degradation in switching speed that will occur as a function of the number of analog switches driven — that is, the fan-out capability.

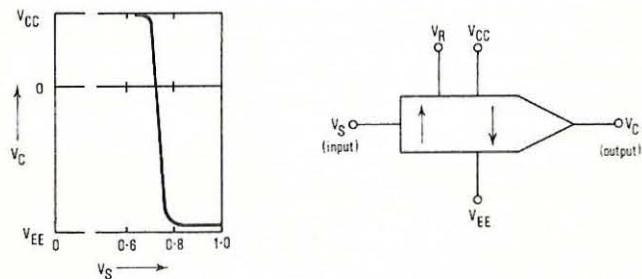


Figure 70 Typical transfer function and symbol for low input voltage driver — e.g. Siliconix D113F or D121F.

7.4 Driver/analog-gate combinations

The final step in analog-switch technique is obviously the inclusion of drivers and analog switches in the same microcircuit. From the foregoing it is clear that the number of possible combinations is enormous, so that it would be pointless to single out a few for discussion. Instead Figure 71 has been included to illustrate

(a) the type of circuitry found in driver/gate combinations, (b) some of the functions available in multiple driver/gate microcircuits and (c) a selection of typical applications.

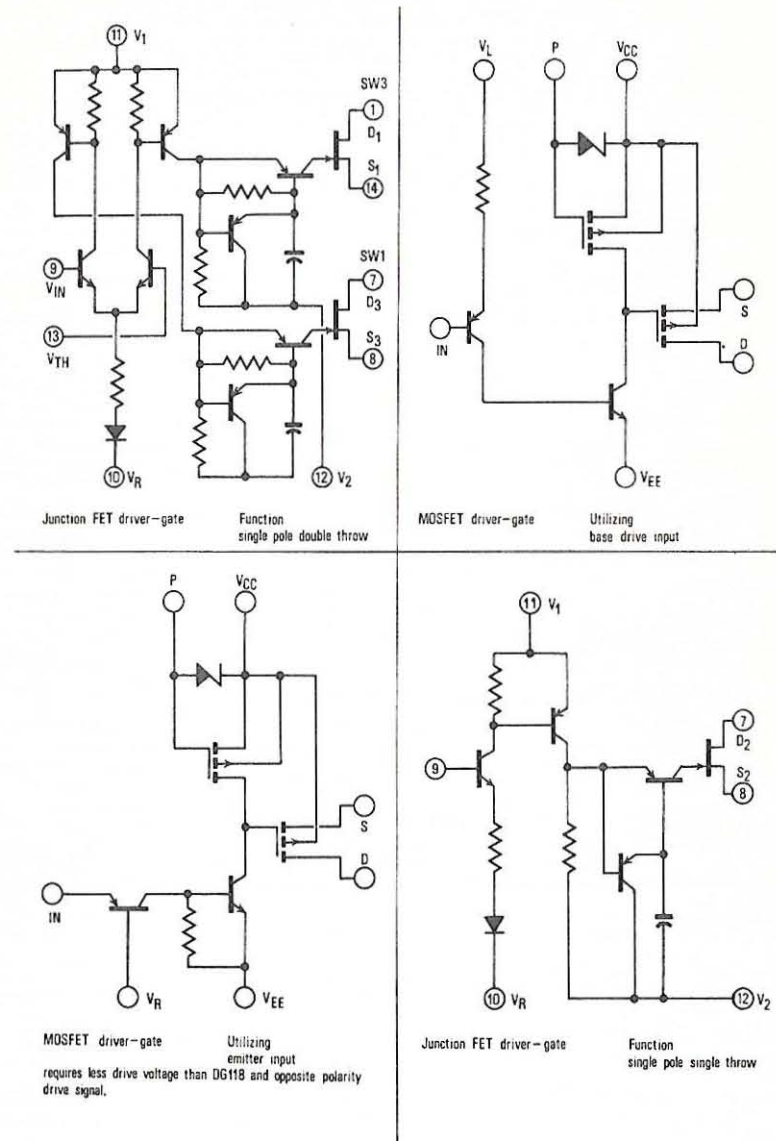


Figure 71a Typical circuit configurations for driver/gate combinations.

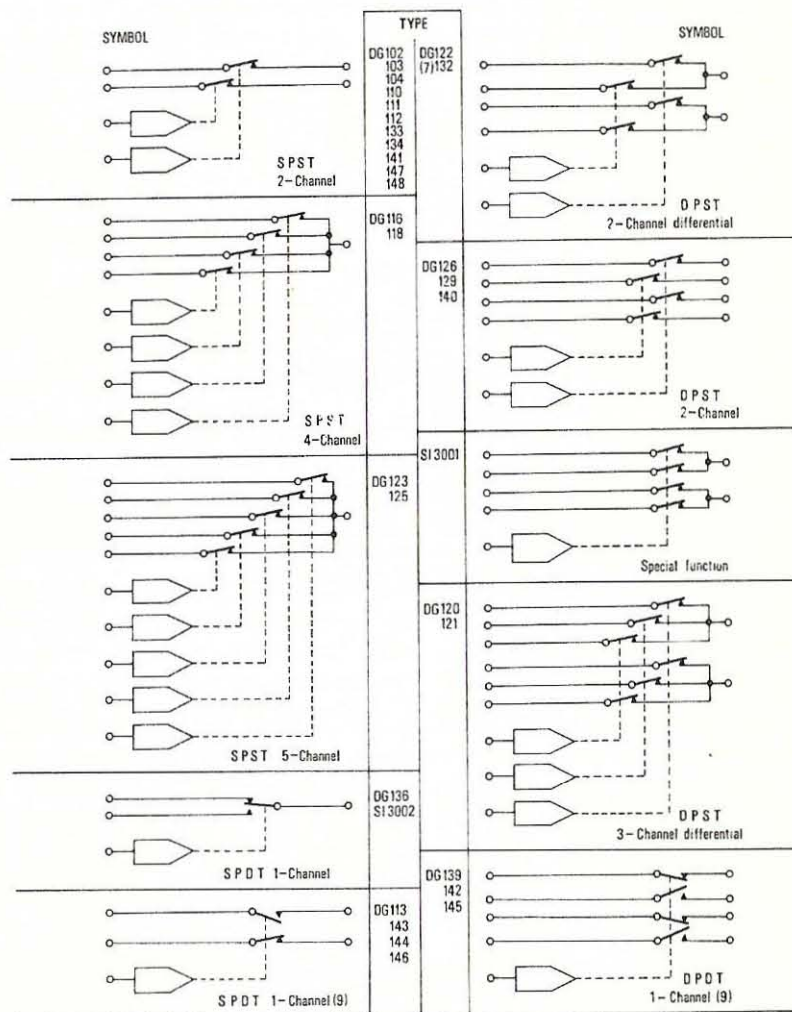


Figure 71(b) Typical examples of driver/gate combinations.

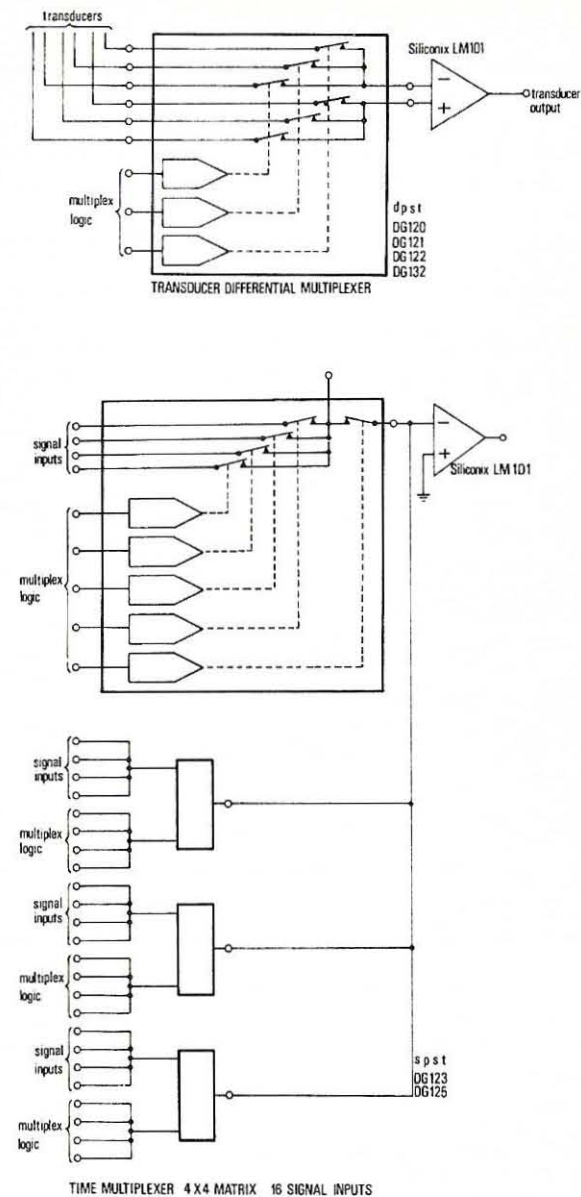


Figure 71(c) Some applications of integrated driver/gate units

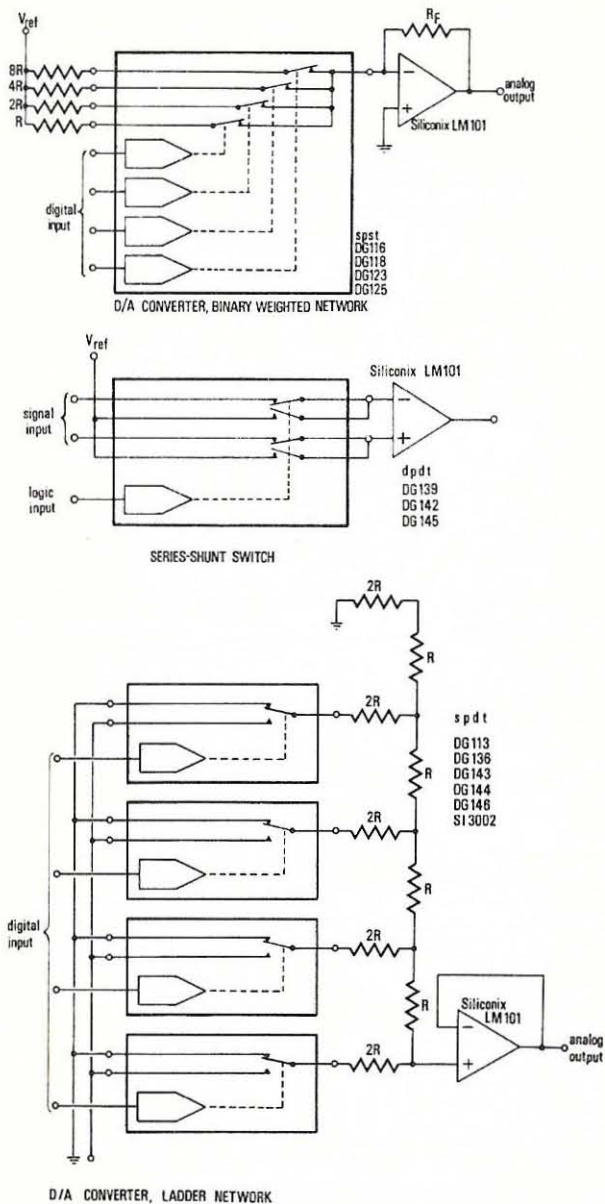


Figure 71 (c) cont. Some applications of integrated driver/gate units.

7.5 The linear monolithic microcircuit

It is now possible to integrate field-effect and bipolar structures, and the Siliconix L120 dual amplifier consists of two integrated amplifiers, one circuit of which is shown in Figure 72. Here the input device is a dual MOSFET connected as a difference amplifier, the common sources of which are supplied from a bipolar constant-current assembly. One drain has a bipolar temperature-compensated 'active' load, and the output feeds a bipolar common-emitter stage which has a MOSFET 'active' load — also temperature-compensated.

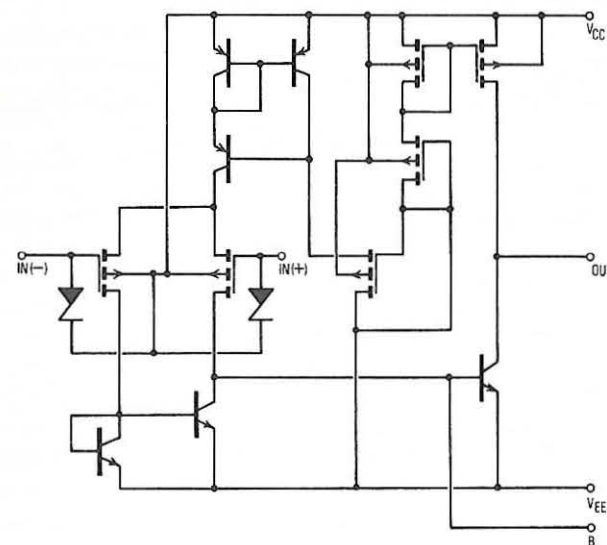


Figure 72 The Siliconix L120 linear integrated amplifier circuit.

The amplifier has quite a low open-loop gain within the range 100 - 1000, and is intended primarily for closed-loop unity-gain applications, such as the sample-and-hold circuit of Figure 73. Here the very low input leakage (less than 50 pA at 25°C) is of particular importance, as it represents an input resistance of some 2×10^{11} ohms. The L120 is inherently stable at unity gain, and has a slewing rate of 20V per microsecond: which attributes make it useful as a fast voltage comparator.

For the unity-gain application, the output is simply connected to the inverting input, and this provides bias for the inverting gate. If, however, a filter which has a d.c. path through it (such as a Twin-T) is inserted into the lead, a useful frequency-selective amplifier will result.

Figure 73 *Siliconix L120 dual integrated amplifier as dual unity-gain amplifiers, or buffers.*

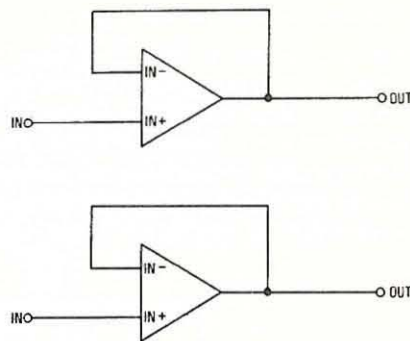
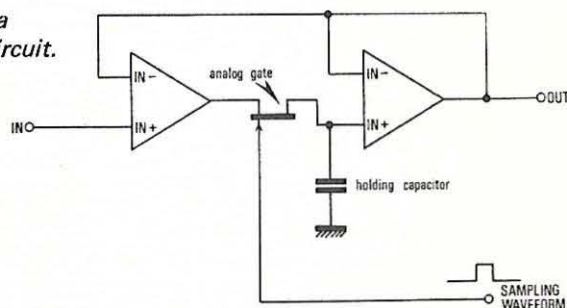


Figure 74 *The L120 used in a sample-and-hold circuit.*



The L120 may be considered the forerunner of linear high input impedance monolithic i.c.'s which will, in due course, become competitive with the hybrid or multi-chip units which at the time of writing are paramount.

Chapter 8

MISCELLANEOUS DEVICES AND APPLICATIONS

8.1 Introduction

Previous chapters have briefly covered the most common field effect devices and their areas of application. There are, however, other devices and applications: the latter continuing to proliferate as designers become increasingly aware of the potentialities of the field effect structure. For this reason this handbook concludes with a small selection of topics not falling naturally into the categories discussed earlier.

8.2 The photo-FET

When energy in the form of heat or light is applied to semiconductor material, the number of electrons in the valence band which acquire sufficient energy to jump the first conduction band increases. The resultant free carriers are then available for current conduction; that is, intrinsic conduction increases (as opposed to extrinsic conduction which depends on the doping level). When a reverse-biased junction is present — as in a FET — the free intrinsic carriers are accelerated across the depletion layer to produce the leakage current. This is why the leakage current is a function of temperature. It also explains why, when the encapsulation of a FET is arranged to permit the entry of light, a photo-detector results¹⁹

Figure 75 (a) shows a N-channel photo-FET (i.e. the Siliconix P236, P237 or P238) connected as a source-follower. The biasing system is normal, and implies that a quiescent current I_Q flows under dark conditions as defined by the bias diagram of Figure 75 (b). The bias-line on this diagram will be seen to cut the V_{GS} axis at a small positive voltage. This is the voltage drop across R_G due to the small leakage current I_G :

$$V_B = I_G R_G \quad \dots (8.1)$$

When the photo-FET chip is illuminated via the lens (which forms the end of the TO-18 can), this leakage current increases by an amount I_p , the photo-current.

Hence

$$V_B = (I_G + I_p) R_G \quad \dots (8.2)$$

The photo-current is directly proportional to the intensity of the incident light (for a constant color content) and clearly results in a voltage drop which increases the drain current over and above I_Q . The circuit is therefore exactly comparable

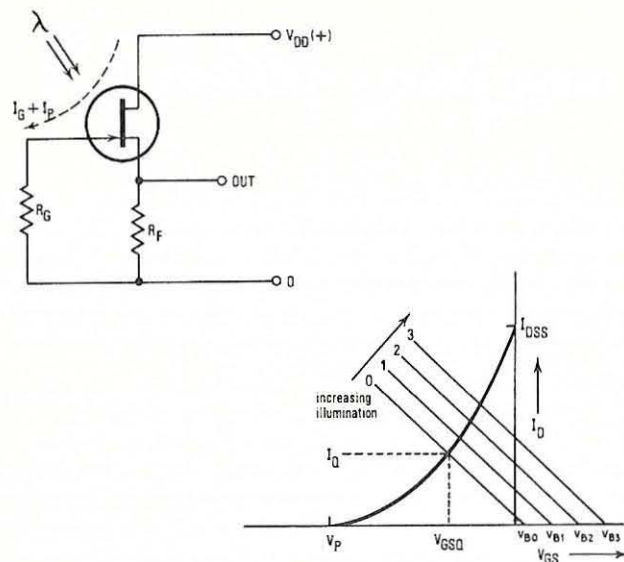


Figure 75 (a) The Photo-FET connected as a source-follower, with (b) bias diagram showing rise of operating point with increasing illumination

to a source-follower stage with a voltage input signal, and because R_F is a feedback resistor, its tendency is, as usual, to linearize the stage. Thus V_{out} is directly proportional to the incident light intensity within the limits of linearity normal to a source-follower.

In equation 8.2 it will be seen that the leakage current I_G (which approximates to I_{GSS}) contributes to the voltage drop across R_G , and hence to the output voltage. This means that the output will be independent of the leakage current only if:

- (i) $I_P \gg I_G$
- (ii) the quiescent output voltage is backed-off by a standing voltage (preferably the quiescent output voltage of a matched stage having its photo-FET kept dark)
- and (iii) the incident light is chopped so that the resultant a.c. output may be taken off via a capacitor.

Condition (i) is usually relevant to ON/OFF applications such as punched tape or card readers, where the illumination level can be quite high.

Condition (ii) is that under which simple photometers operate, and two examples are given in Figures 76(a) and 76(b). Here Siliconix P102 P-channel FET's have been used.

Figure 76a Simple photometer.

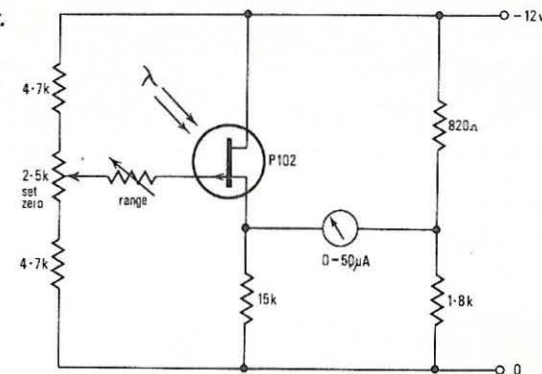
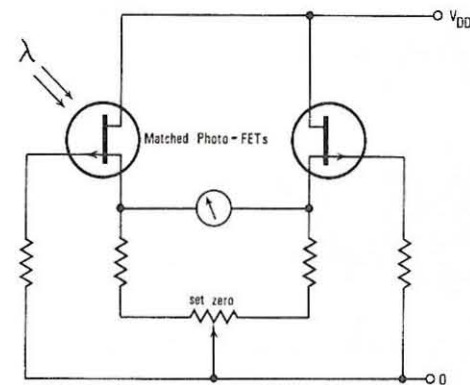


Figure 76b Drift-balanced photometer.



The detection or measurement of a chopped light beam involves the simplest mode of operation, drift being unimportant, and the photo-FET may, if desired, be incorporated as the first stage of a feedback amplifier in the usual way. Thus a linear high-gain amplifier can be constructed, having a light rather than a voltage input signal.

The sensitivity of the photo-FET is a function of both the intensity and the spectral content of the incident light. It is usual to quote this sensitivity in terms of the gate photocurrent, so that variations in the FET parameters or in the external circuit do not become involved.

For example, the sensitivity of the Siliconix P102 is (typically):

$$S_I = 1.2 \mu A/mW/cm^2 \text{ for radiation at } 0.9 \text{ microns}$$

This means that when radiation of 0.9 microns (9000\AA), which is in the near infra-red, falls on the photo-FET, the gate current will be $1.2 D_R$, where D_R is

the irradiation in milliwatts per square centimeter. Hence the equivalent input voltage is:

$$\Delta V_{GS} = S_I D_R R_G \quad \dots (8.3)$$

The Noise Equivalent Power, or N.E.P., is defined as the level of irradiation which would produce a signal voltage equal to the noise voltage under the same external conditions. That is; the level of irradiation at which the signal-to-noise ratio is unity.

Both signal and noise voltages can be referred to the input, or gate, both being subject to the same amplification, so that N.E.P. may be given by:

$$N.E.P. = \frac{v_N \cdot A}{S_I N R_g} \quad \dots (8.4)$$

where v_N is the total input noise voltage due to both \bar{e}_n and the thermal noise of R_g ; and A is the effective area of the device.

As an example, consider the P-102 operating with a 0.9 micron light beam (from a gallium arsenide diode lamp) chopped at 100 Hz. The data sheet curves of v_N versus frequency give a value of $0.2 \mu V / \sqrt{Hz}$ when $R_g = 1$ megohm; and A may be assumed to be $7.9 \times 10^{-2} \text{ cm}^2$. Hence, from equation (8.4):

$$N.E.P. = \frac{0.2 \times 7.9 \times 10^{-2}}{1.2 \times 10^6} = 1.32 \times 10^{-8} \text{ mW} / \sqrt{Hz}$$

(Note: for bandwidths other than unity, the term Δf must be included in the denominator).

A very common figure-of-merit is the detectivity, D^* , which is defined as the unity bandwidth signal-to-noise ratio for a photodetector of unit effective area irradiated with unit power. That is,

$$D^* = \frac{S_I \cdot R_g}{v_N}, \quad \dots (8.5)$$

and observing that the N.E.P. for a cell of unit effective area is simply $v_N / S_I R_g$, this becomes:

$$D^* = \frac{1}{N.E.P.}$$

The signal-to-noise ratio for any photo-detector is proportional to the root of the effective area, so that for a cell of area A ,

$$D^* = \frac{\sqrt{A}}{N.E.P.} \quad \dots (8.6)$$

For the P-102 working under the same conditions as in the foregoing example, the detectivity may be calculated:

$$D^* = \frac{7.9 \times 10^{-2}}{1.32 \times 10^{-11}} = 2.3 \times 10^{10} \text{ cm} \cdot \sqrt{Hz/W}$$

8.3 The FET squaring circuit

In some areas of signal processing — such as noise and power measurement for example — the squaring of a waveform is desirable. Here the square-law transconductance characteristic of the junction FET is particularly useful, for if two matched FET's are driven in antiphase by an input signal, then the sum of the two drain currents will consist almost entirely of a square wave component plus the quiescent current:

If

$$V_{GS(1)} = V_{GSQ} + v_{gs}$$

and

$$V_{GS(2)} = V_{GSQ} - v_{gs}$$

then

$$i_{D(1)} + i_{D(2)} = I_{DSS} \left[\left(1 - \frac{V_{GSQ} + v_{gs}}{V_P} \right)^2 + \left(1 - \frac{V_{GSQ} - v_{gs}}{V_P} \right)^2 \right]$$

$$= \frac{2I_{DSS}}{V_P} \left[(V_P - V_{GSQ})^2 + v_{gs}^2 \right] \quad \dots (8.7)$$

The basic squaring circuit, and the composite transconductance characteristics, are sketched in Figures 77(a) and 77(b). The resultant departs slightly from the ideal parabolic form because the two separate transconductance curves are, of course, only approximate square-laws. This leads to a certain amount of distortion in the output signal, which is further degraded by the phase-splitter (see Figure 78) which must exist if the original input signal is single-ended.

Figure 77a shows that the output voltage is dropped across a load resistor connected to the commoned drains. If the signal frequency is sufficiently high,

Figure 77a Basic squaring circuit.

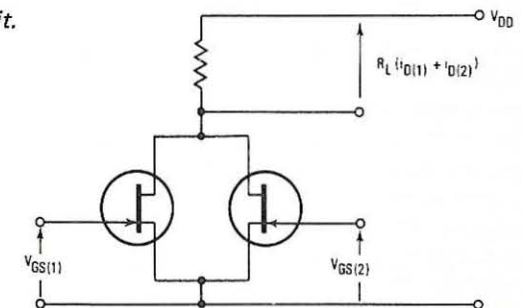
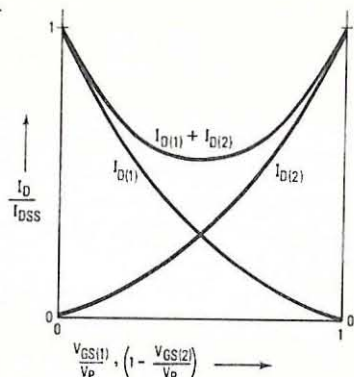


Figure 77b Composite transconductance characteristics for the squaring circuit of Figure 77a.



the output may be extracted via a capacitor connected to these drains. But for very low frequency signals, d.c. techniques must be used, which means that considerable attention must be paid to drift compensation in the circuit. The optimum devices for this application are the Siliconix 2N4867 single or 2N5519 dual series, due to that fact that they most closely obey the square law transconductance curve.

Although it has been assumed that FET's must be matched for successful squaring, in fact this is not necessarily so. Reference ²⁰ available from Siliconix Limited shows how unmatched FET's may be employed if balancing procedures and components are included.

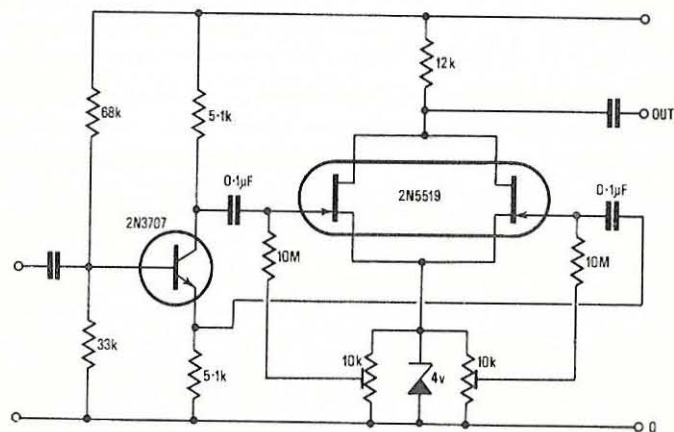


Figure 78 Simple squaring circuit with phase splitter.

8.4 Regenerative switching circuits

The three fundamental regenerative switching systems in electronics are the astable, monostable, and bistable configurations — all of which are variations on the theme that when one active device turns ON, it switches the other OFF in the process, and vice versa. As the names suggest, the **astable** circuit is free-running, and will produce a square-wave; the **monostable** needs an external stimulus to switch it over, when after characteristic dwell-time it reverts to the stable state; and the **bistable** circuit needs an external stimulus to switch it both over and back.

The low base-emitter voltages of the bipolar transistor makes it very suitable for the majority of regenerate switching circuits; but for certain specialized applications, such as long dwell-time circuits, FET's become preferable. Figures 79 and 80 illustrate astable and monostable circuits, each of which has a dwell-time of the order of half-a-minute.

Both examples depend on the fact that the capacitor slowly charges through the 10 megohm resistor without significant leakage via the gate of the FET. (The capacitor itself must, of course, also be a low leakage component).

In the case of the astable circuit, close equality of dwell-times depends upon the closeness of match of

- the pinch-off voltages for the FET's
- the two capacitances
- the two resistances

and

Figure 81 shows a bistable circuit²¹. Here the advantage is not related to the high input resistance of the FET, but to its low power consumption capability. For the circuit shown power consumption is only some 180 microwatts.

Finally, Figure 82 has been included to show how a photo-FET may be used in a regenerative latching circuit. This circuit will turn ON when a pre-determined level of illumination is reached, after which a manual reset is required. Such a circuit could be of use in a flame-detector circuit, for example.

8.5 Oscillators

The high input resistance of the FET has already been shown to be useful in astable regenerative oscillator circuits where a long dwell-time is required (Figure 79). The same high input impedance facility is also useful in sinusoidal oscillator circuits which include feedback elements and which must feed (ideally) into infinitely high load impedances. Cases in point include the conventional Twin-T and Wein-Bridge networks, and an example of the latter is included in Figure 83. Here the Wein network is fed from the low impedance output of the emitter-follower, and is loaded by the very high impedance presented by the gate of the FET. The biasing of the FET is easily accomplished by taking the 'ground' end of the Wein network to a Zener diode.

Figure 79 *Astable circuit (multi-vibrator) for one cycle per minute (approx.)*
(Note: Capacitors must be very low leakage, non-polarized).

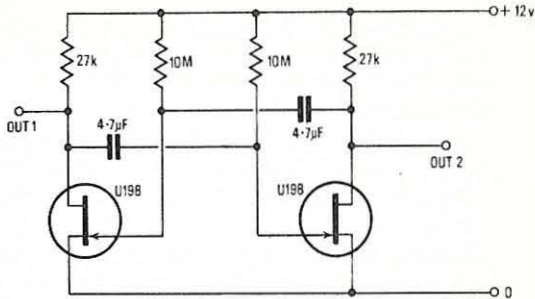


Figure 80 *Monostable circuit*
Dwell-time approx. half-minute with 10MΩ resistor and 2µF capacitor shown.

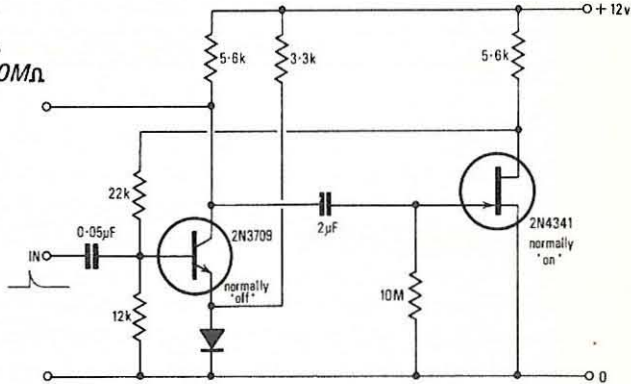


Figure 81 *Very low power bistable circuit. Dissipation approx. 180 mW, trigger approx. +7.5V.*

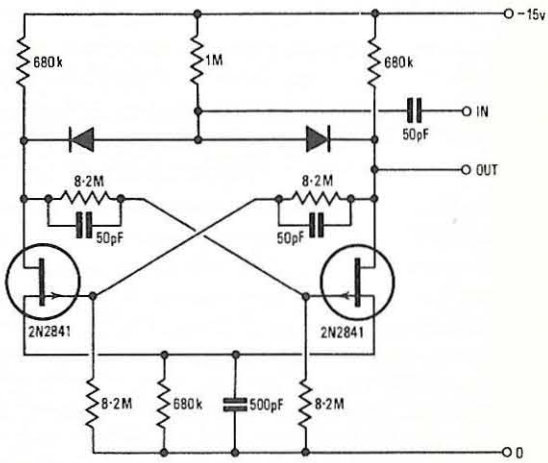


Figure 82 *Photo-FET latching circuit.*

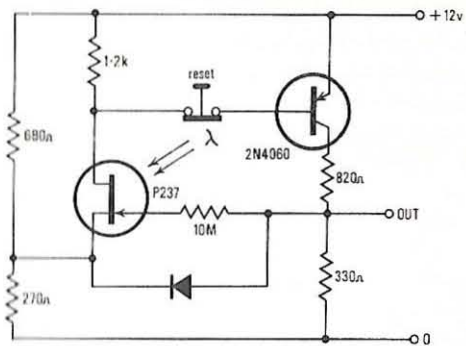
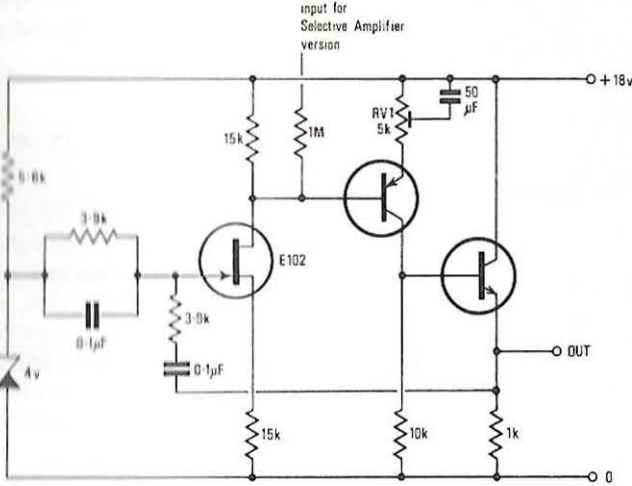


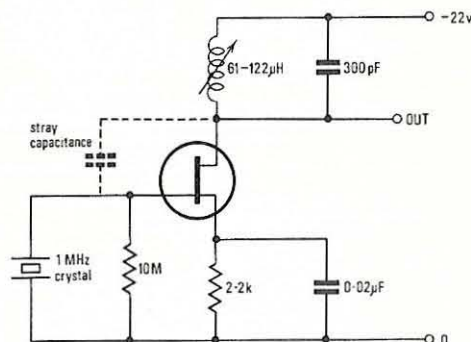
Figure 83 *Wein Bridge oscillator/selective amplifier. (Wein components shown give 400 Hz center frequency).*



Note that if the forward gain of the amplifier is reduced to below three, then because the attenuation in the Wein network is also three, the loop-gain will become less than unity, and oscillation will cease. (This may be achieved by introducing degeneration into the common-emitter stage; that is, by using RV1 to allow part of the emitter resistor to remain unbypassed). The circuit then becomes a frequency-selective amplifier, having a Q which is controllable (also by RV1). The input signal may be injected at the base of the CE stage and extracted at the emitter of the emitter-follower.

Other forms of FET oscillator follow bipolar practice quite closely. For example, a crystal oscillator may be very simply built as shown in Figure 84²². Here the use of a FET results in good Q because the gate circuit does not significantly load the crystal itself.

Figure 84 1 MHz crystal oscillator.



8.6 Conclusion

This book has been published to give a brief outline of the potentialities of the family of field effect transistors. The circuits depicted are basic; that is, they contain only the minimum of components necessary for operation, and it has been left to the reader to modify and incorporate them in the light of experience into more sophisticated networks. Such circuits are necessarily transient, for as the number of devices — both discrete and i.c. FET's — continues to grow, so will the best, cheapest or most reliable method of achieving a desired result not remain constant. Siliconix continually introduce new devices, and maintain a comprehensive flow of data sheets and application reports to enable the designer to remain fully informed of the latest advances in field effect electronics.

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Symbols and Definitions

		Page of first occurrence
BVDGS	Maximum drain-gate voltage with source s/c to drain	21
BVDSS	Maximum drain-source voltage with gate s/c to source	21
BVDSX	Maximum drain-source voltage with specified gate bias	21
BVGSS	Maximum gate-source voltage with drain s/c to source	20
C_{ds} (or C_{rss})	Drain-source capacitance	26
C_{gd}	Gate-drain capacitance	26
C_{gs}	Gate-source capacitance	26
C_{iss} (or C_{gss})	Gate input capacitance with drain s/c to source	28
C_{oss} (or C_{dss})	Drain output capacitance with gate s/c to source	28
CMR	Common-mode rejection ratio	72
g_{fs}	Transconductance	18
g_{fso}	Transconductance when $V_{GS} = 0$	18
g_{os}	Output conductance	21
I_{CL}	Current passed by saturated current-limiter	65
i_d	Incremental drain current	27
I_D	Direct drain current	7
I_Q	Quiescent value of drain current	39
I_{DSS}	Drain current when $V_{GS} = 0$	7
I_{DGO}	Drain-to-gate leakage current when source is o/c	23
$I_D(ON)$	Drain current for specified (ON) bias conditions	29
$I_D(OFF)$	Drain current for specified (OFF) bias conditions	23
I_G	Gate leakage current	39
I_{GSS}	Gate leakage current when drain is s/c to source	13
NF	Noise factor	49
R_D	Drain resistor	34
R_F	Feedback resistor	43
R_L	Load resistance	40
R_S	Source resistor	33
r_{ds}	Incremental channel resistance	21
r_{DS}	Chord or large-signal channel resistance	22
r_{gd}	Gate-drain resistance	27
r_{gs}	Gate-source resistance	27
T	Temperature	37
V_B	Gate bias voltage with respect to common line (or ground)	33
V_{DD}	D.C. supply rail voltage	36
V_{DS}	Drain-source voltage	7
V_{GS}	Gate-source voltage	8
V_{GSQ}	Quiescent gate-source voltage	8
$V_{GS(th)}$	Threshold voltage (for enhancement MOSFET)	8
V_{ig} V_{ig} V_{og} V_{rg}	Common-gate y-parameters	75, 76
V_{fs} V_{is} V_{os} V_{rs}		
	Common-source y-parameters	75, 76